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Defense Advanced Research Projects Agency
Contracts Management Directorate
3701 North Fairfax Drive
Arlington, VA 22203-1714

Attention: Scott R. Ulrey
Contracting Officer

Subject: Final Technical Report Distribution

Reference: (a) Contract MDA972-91-C-0035, PZ0004

Enclosure: (1) Final Technical Report, 3-D Diamond MCM Technology Development Program
(2) Report Distribution List

Dear Mr. Ulrey:

The final program review and demonstration of the 3-D Diamond Test Bed was successfully completed in November 1998.

The Enclosure (1) final technical report has been distributed to the addresses listed in modification PZ0004 and other addresses as noted in the Enclosure (2) distribution list.

If additional information or clarification is desired, please contact me at 972-206-8522.

Sincerely,

Ken Kagiyama

Kenneth H. Kagiyama
Sr. Contract Administrator

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Contract MDA972-91-C-0035
3-D Diamond MCM Technology Development Program

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3-D Diamond MCM Technology Development Program

Final Technical Report

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30 November 1998

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13. ABSTRACT *(Maximum 200 words)*

3-D Diamond MCMs is an enabling technology to support chip-to-chip and module-to-module high-density connectivity and thermal management. The extremely high conductivity of diamond, coupled with its electrically insulating nature, makes it an ideal choice for solving 3-D packaging problems. The thermal conductivity is so high as to allow over 80 W/in^{3}of power dissipation to be extracted from a stack of diamond substrates by lateral thermal conduction techniques alone. Diamond laterally conducts the heat generated by the logic out of the "battle zone" of the actively populated 3-D stack of MCMs. This frees the designer to fully utilize all of the space between boards to implement a high area density array of vertical z-axis interconnects between all adjacent boards in the stack to minimize interconnect delays. This report summarizes the design, fabrication, integration and testing of a Demonstration Test Bed that was utilized as a tool for testing and demonstrating the thermal management capability of diamond MCMs. A signal integrity analysis was also performed to illustrate the high speed signal viability through the z-axis 3-D interconnect structure itself. Supporting system design details, photographs of fabricated components and subsystems, and test results are provided.

14. SUBJECT TERMS

3-D Diamond Multichip Module (MCM)

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1. INTRODUCTION

Artificial diamond substrates, produced by state of the art chemical vapor deposition (CVD) techniques, have unsurpassed thermal conductivity properties, extremely low coefficients of thermal expansion, and are able to withstand high processing temperatures. Assuming that its cost can be brought low enough, diamond offers a promising solution to many difficult electronic packaging problems. For example, the multi-chip module (MCM) approach for achieving very high chip packaging densities is of particular interest for high performance, high clock rate digital systems, where signal latency due to excessive inter-chip interconnect line lengths can prove a major limitation.

As IC chips are operated at higher frequencies, their power dissipations tend to increase proportionally. As these chips are jammed together very closely in MCM packaging, the power density levels get very high indeed. These severe thermal management problems represent a serious barrier to the application of MCM technology in high performance systems.

Diamond, which has the highest thermal conductivity known, has been used as a heat sink material in critical device applications for many years. Only recently, however, has the promise of major reductions in the price of diamond allowed its consideration for use in electronic thermal management situations such as MCMs. Such applications require many tens of grams, rather than milligrams, of diamond material.

The combination of high thermal conductivity with an electrical insulating nature makes diamond an ideal packaging and MCM substrate material. In addition to its capability for reducing chip temperatures in conventional packaging configurations, diamond can make it practical to implement more efficient advanced 2-D packages, as well as ultra high performance, 3-dimensionally interconnected MCM packaging approaches.

To that end, the Defense Advanced Research Projects Agency (DARPA) is committed to decreasing the amount of development time required for inserting diamond substrate technology into fielded electronics systems. Raytheon Systems Company, with subcontractors Cray Research, Inc., Norton Company, and Isothermal Systems Research, Inc., is under DARPA contract to:

a) Develop and demonstrate diamond substrate fabrication technology.

b) Develop, demonstrate and characterize two-dimensional (2-D) Diamond Multichip Modules (MCM-D).

c) Develop, demonstrate and characterize 2-D Diamond/Laminate Printed Circuit Board (PCB) technology.

d) Develop, demonstrate and characterize three-dimensional (3-D) Diamond MCM-Ds.

e) Develop and demonstrate an efficient heat removal system for the 2-D and 3-D MCM technology

An underlying theme of the effort is to perform the diamond MCM technology development within the emerging MCM commercial infrastructure so as to make the technology available for both military and commercial microelectronics systems.

1.1 Program Goals

The major objective of this program is to shortcut the time it takes the US to get leading diamond substrate technology into electronic system applications via 3-D diamond MCM and advanced PCB architectures. In response to this objective, this program consisted of a systematic, multitask approach to meet the following specific goals:

(1) Develop and demonstrate diamond substrate fabrication technology that will support diamond MCM fabrication, as well as provide for a highly thermally conductive substrate for advanced PCBs.

(2) Perform real world system demonstrations of the effectiveness of 3-D diamond substrate technology.

Raytheon Systems Company, Garland Operation (RSC-Garland), performed as the prime contractor and provided overall project coordination, systems engineering, and military application guidance, and military demonstration system design and test. RSC-Garland additionally provided lead engineering for development of a 3-D diamond additive process MCM (MCM-D).

Cray Research, Inc., as a major subcontractor, led the development around diamond enhancements of a laminate PCB technology.

Norton Diamond Film, as a major subcontractor, served as a commodity diamond substrate vendor for MCM and laminate PCB applications.

Isothermal Systems Research (ISR), Inc., as a subcontractor to RSC-Garland, performed the analysis effort, design, and fabrication of a spray cooling thermal management apparatus to support test demonstrations.

General Electric Corporate Research and Development (GE/R&D) provided material and process verifications of multi-layer electrical interconnect depositions on diamond substrates, and fabricated the final diamond MCMs utilized in the 3-D Diamond MCM Demonstration Test Bed.

1.2 Program Tasks

Four basic tasks were funded by DARPA under this program to accomplish these goals and are identified as follows:

Task 1A

- Perform thermal, mechanical, electrical, signal interconnect, and power management designs for both 2-D and 3-D diamond MCM and laminate/PCB Demonstration Test Beds that emulate very high performance digital systems
  - Operating frequencies up to 1 GHz should be considered
- Perform a design trade-off for an Airborne Military Processor assessing the size, weight and performance advantageous of 3-D MCM technology in military roles

Task 1B

- Develop basic large-scale diamond substrate manufacturing technologies including:
  - Cutting and finishing (top, bottom. and edges)
  - Thru-substrate via laser drilling, metallization, and planarization
  - Power plane metallization (top, bottom, edge contacts)
  - Multi-layer (metal/dielectric) interconnect technology
  - Die attach and lead bonding techniques

Task 2

- Develop and test 2-D technology demonstration vehicles
  - Build single 2-D diamond MCM for noise margin, crosstalk, and signal propagation evaluations
  - Build diamond laminate/PCB brass board for noise margin, crosstalk, and signal propagation evaluations

Task 3

- Develop and test 3-D technology demonstration vehicles
  - Build 2-D+ diamond laminate/PCB Test Bed for thermal, mechanical, and signal integrity evaluations
  - Build 3-D diamond MCM Demonstration Test Bed for thermal, mechanical, and signal integrity evaluations

By pioneering the development of diamond substrate 3-D MCM technology, clearly defining the design rules for its use in high speed electronics, and demonstrating its effective size, weight, and performance advantage over conventional 2-D systems, this program should paint the way for the widespread use of this technology.

1.3 Program Schedule

This program was initiated in October 1991. Figure 1-1 displays the original 42 month master schedule outlining the sequential performance periods for the program tasks highlighted in the

previous section. The activities for RSC-Garland and each of the major subcontractors are displayed on this figure.

A key task in this program is to demonstrate basic diamond MCM substrate fabrication technology. These fabrication elements include the application of chip-to-chip routing and interconnect technology utilizing a thin-film (metal-dielectric) additive process. In November 1992, RSC-Garland contracted with Texas Instruments Defense Systems and Electronics Office (TI) to serve as the merchant diamond MCM foundry.

During 1993 and 1994, TI made significant advances plus had some serious setbacks regarding the design and fabrication of High Density Interconnect (HDI) structures associated with the involved diamond substrates. The most serious blow came when TI formally announced that they were going to disengage from the MCM market and close their MCM foundry by 31 December 1995. This placed the completion of the current program in jeopardy.

GE's Corporate Research and Development Center (GE/R&D) agreed to take on the role as the MCM foundry and fabricate and deliver to RSC-Garland the involved diamond MCMs. These diamond substrates will be laminated with mutlilayer interconnect as per process and design details developed by TI, Raytheon, and the other involved 3-D Diamond MCM subcontractors to date.

This recovery plan incorporating GE/R&D was approved by DARPA in 1996. Figure 1-2 shows the revised master schedule with GE's efforts beginning in May 1996 as the alternate foundry source.

GE/R&D delivered four partially functional diamond MCMs to RSC-Garland in January 1998. This delivery allowed RSC-Garland to complete the remaining Task 3 engineering, manufacturing and testing activities associated with the 3-D Diamond MCM Demonstration Test Bed. These activities included:

1. Complete Demonstration Test Bed test plan
2. Populate and assemble the involved MCMs with the test characterization die and de-coupling capacitors
3. Complete assembly and integration of the major hardware elements of the 3-D Diamond MCM Demonstration Test Bed
4. Perform a final system check-out of the Test Bed
5. Conduct the required mechanical, thermal, and electrical tests per test plan
6. Perform a formal demonstration of the Test Bed at Garland, Texas in concert with the Government
7. Develop and deliver the program Final Report.

Figure 1-3 provides this schedule highlighting the key Task 3 activities performed by RSC-Garland.

1.4 Scope of Final Report

This Final Report outlines and describes the packaging design, fabrication development, and results of some experimental tests conducted on the 3-D Diamond MCM Demonstration Test Bed. All developments and results presented in this report are based upon RSC-Garland's engineering, fabrication, and testing activities performed under program Task 3 as outlined in the previous section. Contributions made by the involved subcontractors can be found in various related technical reports, interim quarterly reports, and conference papers as listed in following Section 2.0.

Section 3.0 on transferable technology presents a size, weight, and performance comparison of a 3-D MCM structure over a conventional 6U VME card cage. These results suggest that high performance digital signal processing machines normally confined to a computer room environment can be repackaged with this technology for mobile applications.

Section 4.0 provides a summary of the basic accomplishments made by program subcontractors and Raytheon during the performance of this contract. Key 3-D packaging milestones and technolo0gy "firsts" achieved under this effort have been tabulated.

The packaging and performance requirements leading to the ultimate design of the 3-D Diamond MCM Cube Assembly is provided in Section 5.0. Artwork design drawings for the diamond MCMs, fuzz button retainer boards, top and bottom turn-around boards, rigid/flex circuits, and a cube clamping fixture are provided in this section.

Section 6.0 provides brief descriptions of the fabrication processes and procedures for building the Cube Assembly supported by photographs of the final fabricated products.

The design plans and fabrication photographs for the spray cooling assembly (used to extract the heat from the 3-D cube edge) are provided in section 7.0. Special emphasis is given to the design, attachment, and sealing of the spray-cooler plates to the Cube Assembly.

Section 8.0 provides a visual design overview of the test and instrumentation system that was integrated around the Cube Assembly. This system provides the glue and testing tools to implement, report, and summarize the results of select thermal and electrical integrity testing performed on the Cube Assembly.

In Section 9.0, a time domain transient analysis was performed to determine characteristic impedance, signal bandwidth, and time delay for one complete top to bottom interconnect path through all MCM diamond substrates and related spacer boards stacked vertically in the cube computer concept. It is seen that this design of the 3-D stack provides adequate bandwidth and controlled impedance for propagation of digital signals having clock speeds approaching 1 GHz with 60 ps rise and fall times.

Finally, Section 10.0 provides a summary of the effort to carefully model the physical and thermal attributes of the stacked MCMs associated with the Cube Assembly. This model was utilized to verify the critical thermal integrity parameters obtained from comprehensive testing of the Cube Assembly. The principal parameters evaluated by this method included the heat transfer coefficient, H, obtained at the spray-cooled diamond cooling fins at the edge of the diamond substrate MCMs, the die attach thermal resistance, R_{th}(die), and the lateral thermal conductivity, k, of the diamond substrate itself.

Two appendices have been included with this final report in order to provide additional supporting technical information. In Appendix A, the technical role of diamond for use in thermal management applications such as MCMs is identified. Technical examples are developed that show how the excellent lateral thermal conductivity of diamond material can eliminate chip "hot spots" and substantially increase digital system reliability. Technical illustrations are also provided to show how diamond MCMs mounted in a 3-D packaging configuration can get the heat out of the stack utilizing edge-cooling approaches. This frees the designer to utilize the entire active area of the MCMs for high-density vertical interconnects.

Appendix B provides the details of a model of diamond MCM thermal integrity that was developed based upon test results extracted from the completed 3-D Diamond MCM Demonstration Test Bed. The principal thermal parameters evaluated by this method are summarized in Section 10.0. Best-fit values from the collected experimental data are graphed and tabulated in this appendix.

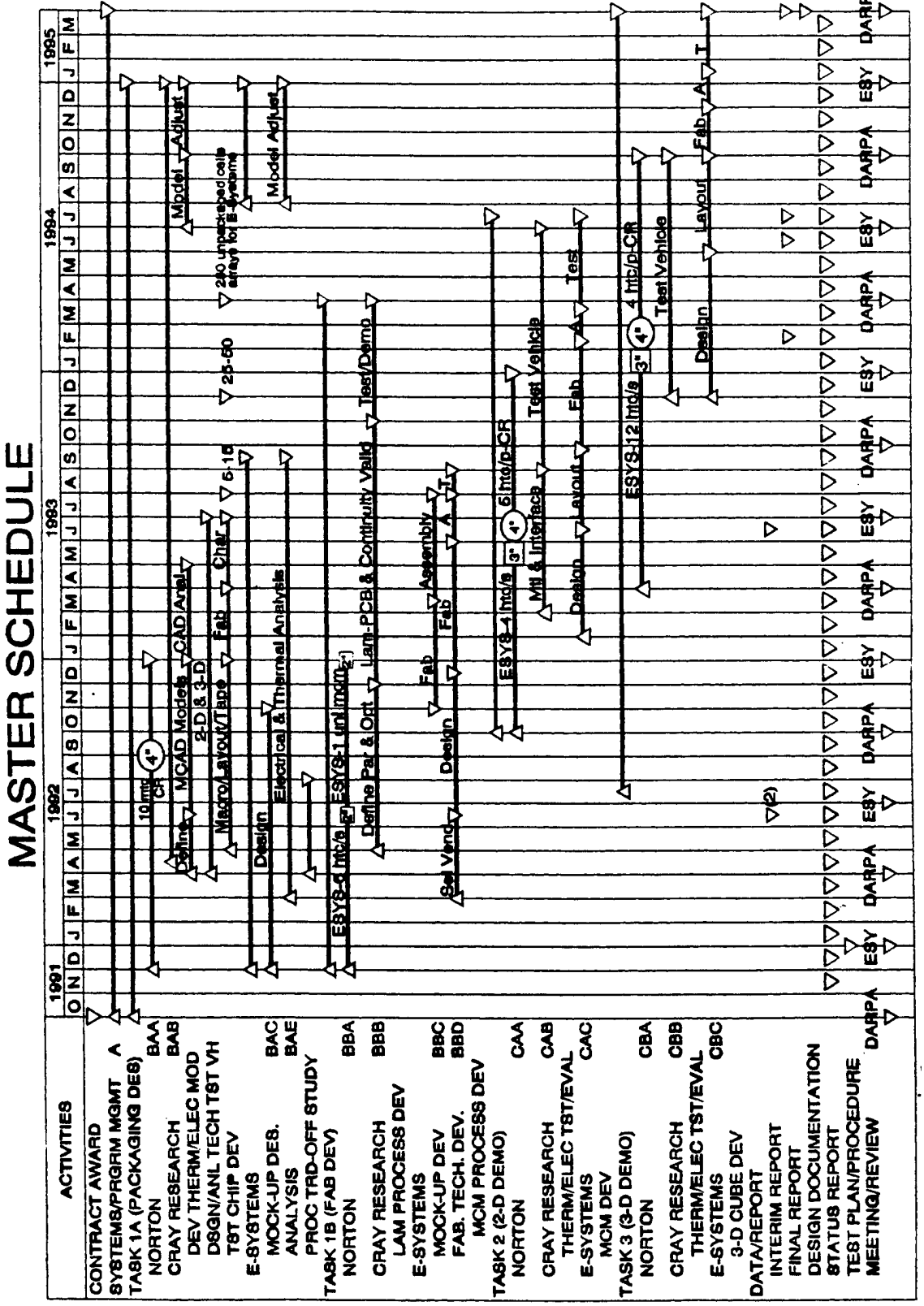


Figure 1-1. Program Master Schedule (October 1991)

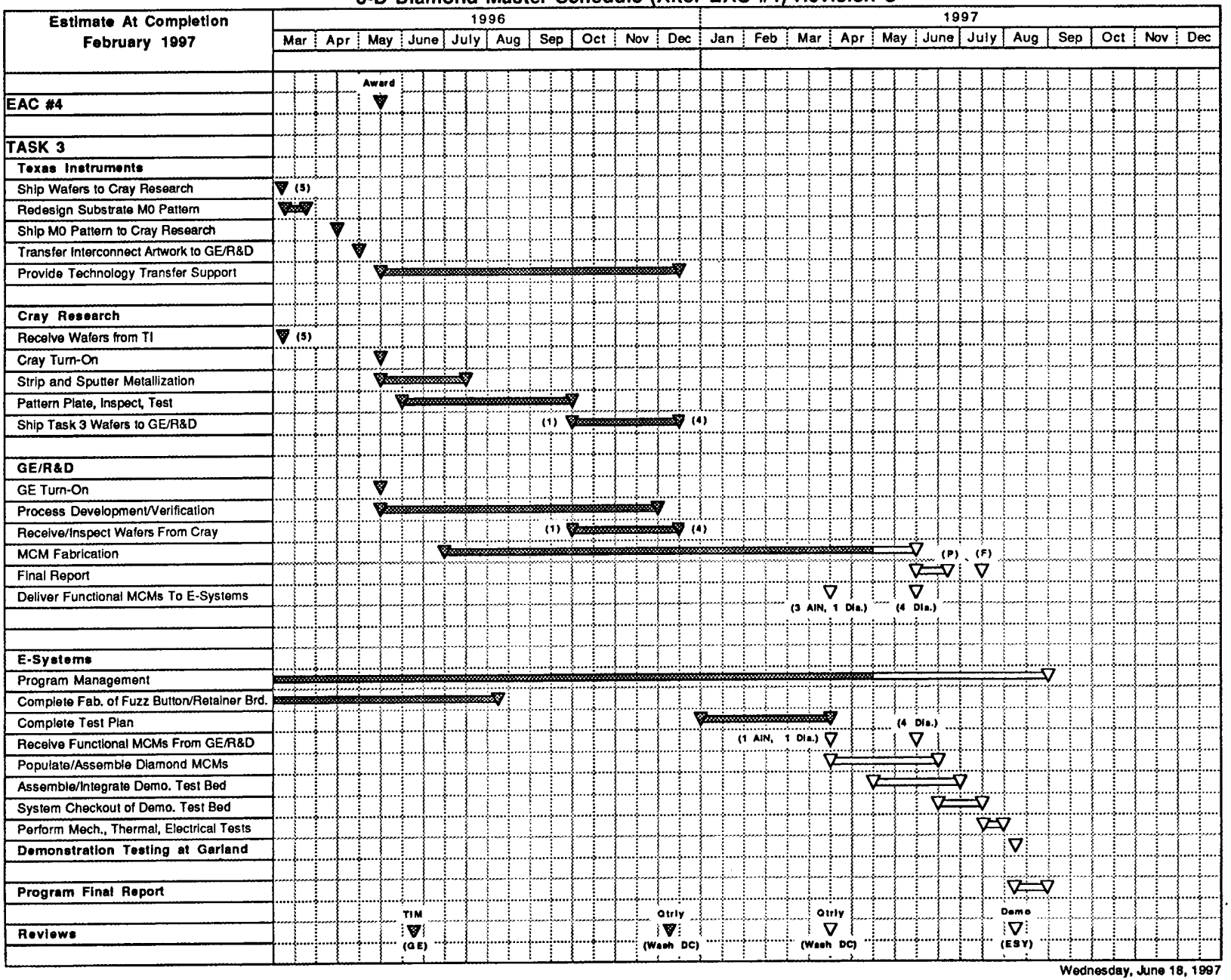


Figure 1-2. Program Master Schedule (Incorporation of GE/R&D)

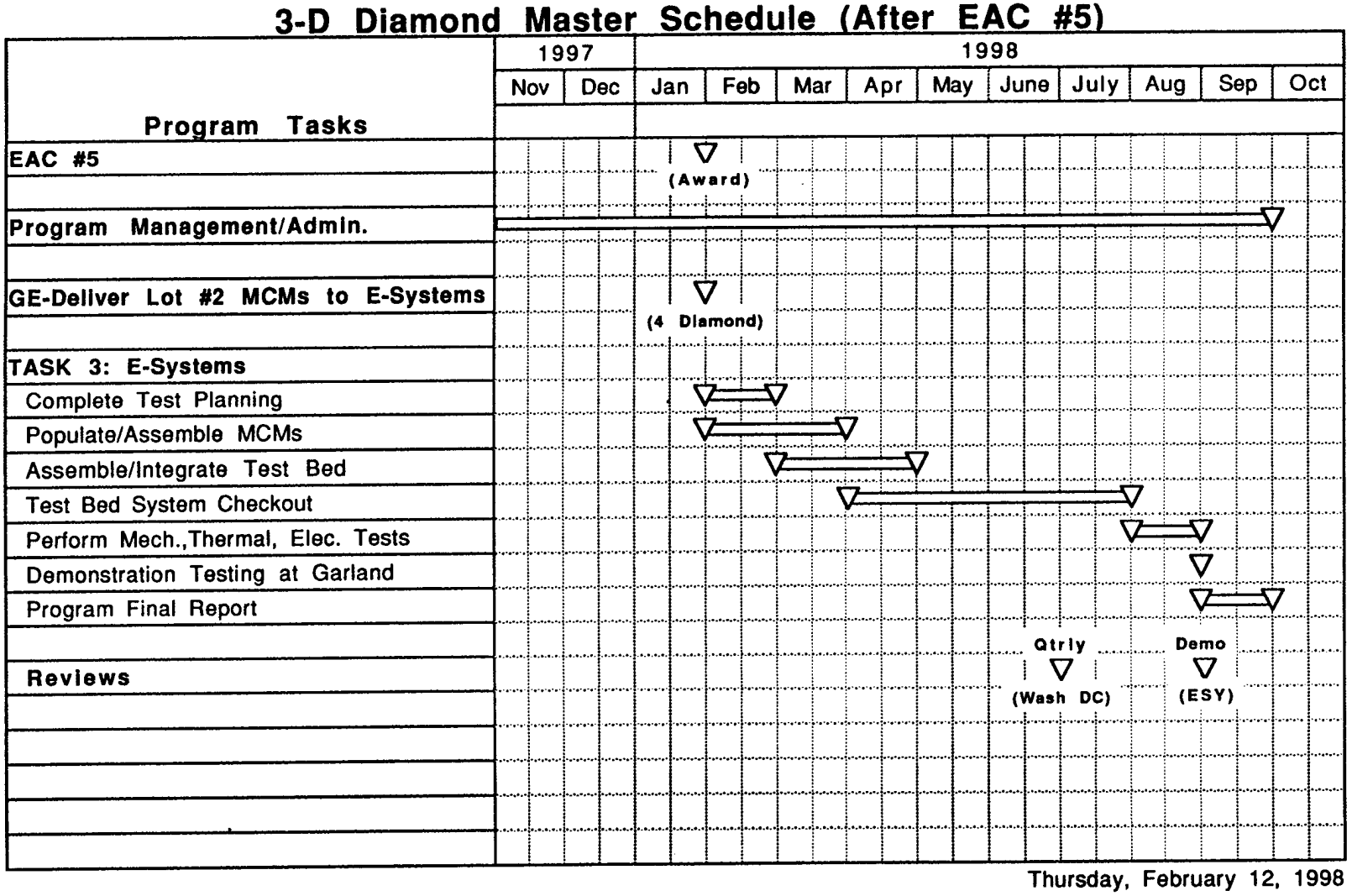


Figure 1-3. Program Master Schedule (Key Task 3 Activities)

2. RELATED DOCUMENTATION

Over the course of Tasks 1A & 1B, and Tasks 2 and 3, a significant number of status reports and technical papers have been generated by Raytheon Systems Company (RSC) and its subcontractors, Cray Research, Texas Instruments (TI), Norton Diamond Film, and Isothermal Systems Research (ISR). The following is a comprehensive bibliography of those reports and papers. In particular, for information concerning the Task 1A and Task 1B efforts and accomplishments of Cray Research and Texas Instruments, please see their Final Task 1A & 1B Reports. The accomplishments of Raytheon are summarized in this Final Report.

Cray Research, Inc.

Control of Blistering of Sputtered/Plated Metallization on Diamond Wafers, ARPA Diamond Report, 1Q94

Control of Blistering of Sputtered/Plated Metallization on Diamond Wafers, Update, ARPA Diamond Report, 2Q94

Metallization Process Specification for Diamond Substrates, ARPA Diamond Report, 2Q94

Diamond Wafer Stress Analysis: Effect of Increased Wafer Bow, ARPA Diamond Report, 2Q94

Thermomechanical Evaluation of Diamond Substrate Assembly, ARPA Diamond Report, 2Q94

Construction of and Thermal Experiments Conducted on DTV3, ARPA Diamond Report, 2Q94

Diamond Wafer Morphology and Adhesion Control of Sputtered/Plated Metallization on TD1309, ARPA Diamond Report, 3Q94

Thermal Analysis of Diamond Test Vehicle #4, ARPA Diamond Report, 3Q94

Failure Analysis of 2D+ Diamond Test Vehicle Laminations, ARPA Diamond Report, 4Q94

Diamond Wafer Stress Analysis: Effect of Increased Wafer Bow, Update, ARPA Diamond Report, 4Q94

Non-linear FEA Analysis of Thermally-Stressed Diamond/Solder/PCB Lamination, ARPA Diamond Report, 4Q94

Summary of Electrical Modeling and Testing Diamond Vias, ARPA Diamond Report, 4Q94

3-D Diamond Project Tasks 1A & 1B Final Technical Report, September 20, 1995

Raytheon Systems Company

3-D Diamond MCM Technology Development Program Monthly Status Reports, March, 1992 through September, 1998 (Total of 79)

3-D Diamond MCM Technology Development Program Quarterly Review, August 20, 1992

3-D Diamond MCM Technology Development Program Quarterly Review, December 2, 1992

3-D Diamond MCM Technology Development Program Quarterly Review, April 21, 1993

3-D Diamond MCM Technology Development Program Quarterly Review, August 31, 1993

3-D Diamond MCM Technology Development Program Quarterly Review, December 8, 1993

3-D Diamond MCM Technology Development Program Quarterly Review,

April 20, 1994

3-D Diamond MCM Technology Development Program Quarterly Review, August 17, 1994

3-D Diamond MCM Technology Development Program Quarterly Review, January 25, 1995

3-D Diamond MCM Technology Development Program Quarterly Review,

April 26, 1995

3-D Diamond MCM Technology Development Program Quarterly Review,

August 30, 1995

3-D Diamond MCM Technology Development Program Quarterly Review,

December 18, 1996

3-D Diamond MCM Technology Development Program Quarterly Review,

June 23,1997

3-D Diamond MCM Technology Development Program Quarterly Review,

May 20,1998

Technical Proposal, Volume 1 for the 3-D Diamond MCM Technology Development Program, 7 March 1991

Cost Proposal, Volume 2 for the 3-D Diamond MCM Technology Development Program, 7 March 1991

Functional Systems Demonstrations, Volume 3 for the 3-D Diamond MCM Technology Development Program, 7 March 1991

Cost Proposal, Volume 2 (Revision A) for the 3-D Diamond MCM Technology Development Program, 18 September 1991

Dual Approach ECP Cost Proposal for the 3-D Diamond MCM Technology Development Program, 25 February 1992

Statement of Work for the Fabrication of Diamond Film Multichip Modules, June 22, 1992

3-D Diamond MCM Technology Development Program: Tasks 1A & 1B Interim Status Report, December 1992

Envelope Drawing, 420-39042, Substrate, MCM, January, 1994

Envelope Drawing, 420-39027, Retainer, Wire Button Contact, May, 1994

Envelope Drawing, 404-00167, Substrate, Aluminum Nitride, January, 1994

Specification, 404-00167, Substrate, Aluminum Nitride, January, 1994

Specification, 404-00166, Substrate, Diamond, CVD, January, 1994

Test Plan, 3-D Diamond Technology Development Program

Texas Instruments Inc.

3-D Diamond MCM Project Task 1B Final Report, August 10, 1994

TI MCM Foundry User's Guide, Version 4.0, including 3-D Diamond MCM Project Task 2 Diamond Design Guide, Rev A, June 30, 1994

3-D Diamond MCM Project, Task 2 and Task 3 Final Technical Report, 23 January 1996

Isothermal Systems Research, Inc.

Spray cooling System Instruction Manual for the Cube Computer Program, November 1, 1994

Technical Papers Presented at Symposiums and Conferences

T. J Moravec, R. C. Eden and D. A. Schaefer, "The Use of Diamond Substrates for Implementing 3-D MCMs," 1993 Proceedings International Conference on Multichip Modules, April 14-16, 1993

D. A. Schaefer, R. C. Eden and T. J. Moravec, "The Role of Diamond in 3-D MCMs," 1993 Proceedings of NEPCON '93, February 11-14, 1993

R. E. Ackerman and D. A. Schaefer, "Wire Button Contact Retainer Board for 3-D Interconnected MCMs," The International Journal of Microcircuits and Electronic Packaging, Vol. 19, Number 4, Fourth Quarter 1996

B. Bartilson, "Heat Transfer Analysis of a 384-Pin Flip-Flop Tab on Diamond Substrate," Engineering Mechanical Research Corporation (E.M.R.C.) Users Conference, Troy Michigan, October 3-5, 1994,

D. Tilton, "Spray cooling for the 3-D Cube Computer," Fourth Intersociety Conference on Thermal Phenomena in Electrical Systems, Washington, D.C., May 4-6, 1994

K. Sienski, R. Eden and D. Schaefer, "3-D Electronic Interconnect Packaging," 1996 IEEE Aerospace Conference, Aspen, Colorado, March 1996

3. TRANSFERABLE TECHNOLOGY

Coupled with their silicon-matched bonding properties and electrical insulator characteristics, artificial diamond substrates are an enabling material technology for implementing extremely high-density microelectronics packaging. Signal latency can be reduced by a factor of 3x over conventional 2-D MCMs through the use of an area array interconnected 3-D configuration. Applications vary from supercomputers through mainframes and high performance workstations.

The technical benefits of this technology include: (1) minimization of interconnect delays in supercomputers operating above 500 MHz, (2) enhancing inter-processor I/O bandwidths in Massively Parallel Processors (MPPs) and scalable processors, and (3) providing for resource additions to workstations such as vector and graphics processors.

From a military standpoint, this technology will lead to new operational capabilities in signal and image reconnaissance systems. From a commercial viewpoint, this technology will accelerate supercomputer and various other computer product developments approaching TERAOPS performance capability.

The benefits of 3-D packaging can be evaluated in terms of size and weight comparison. Table 3-1 contrasts the size and weight advantage of a 3-D MCM structure over a conventional 6U VME card cage. This table contrasts the size and weight of the basic elements of each structure. An element is defined as a printed circuit card for the VME assembly and a single substrate for the 3-D MCM.

Table 3-1. Size and Weight Comparison

Parameter	6U VME	3-D MCM	Reduction
Single Element Weight	**560 g**	**20 g**	**28:1**
Support Structure Weight/Element	**800 g**	**170 g**	**4.7:1**
Single Element Volume	**650 cm^3**	**26 cm^3**	**25:1**
Active Die Area/Element	**32 cm^2**	**16 cm^2**	**2:1**

Calculating from the values in the table, a fully populated 12 card VME chassis will weigh 16.32 kg. The equivalent 24 layer 3-D MCM will weigh 4.56 kg. Similarly, the VME chassis will occupy 7800 cm^3 while the cube will require only 624 cm^3. Therefore, a simple direct replacement will result in a weight reduction of 72% and size reduction of 92%.

Table 3-2 provides a comparison of performance related parameters associated with these two packaging approaches. The 3-D structure offers tremendous improvements in physical connectivity and data transfer rate, both of which contribute to global communication bandwidth.

Table 3-2. Bandwidth and Thermal Performance Comparison

Parameter	6U VME	3-D MCM	Increase
Layer-to-Layer Connections	192	2500	1:13
External Connections/Layer	200	400	1:2
Maximum Power	50 W	500 W	1:10
Layer-to-Layer Data Rate	150 MHz	1 GHz	1:6.7

The increase in power expected with high-speed design is accommodated with an order of magnitude improvement in thermal management capability.

These added design dimensions provide the opportunity for innovative system architectures that are not feasible in current technology. These results suggest that high performance digital signal processing machines normally confined to a computer room environment can be repackaged with this technology for mobile applications. An obvious candidate is an airborne processor used in military applications. Figure 3-1 contains a photograph of a full ATR chassis model enclosing a 3-D cube processor connected to a rack of traditional printed circuit boards. This mock-up represents a full stack of forty 3-D interconnected diamond MCMs with a board-edge spray-cooler for thermal management. Such a 3-D chassis is capable of housing a modern supercomputer in a form factor suitable for embedded applications.

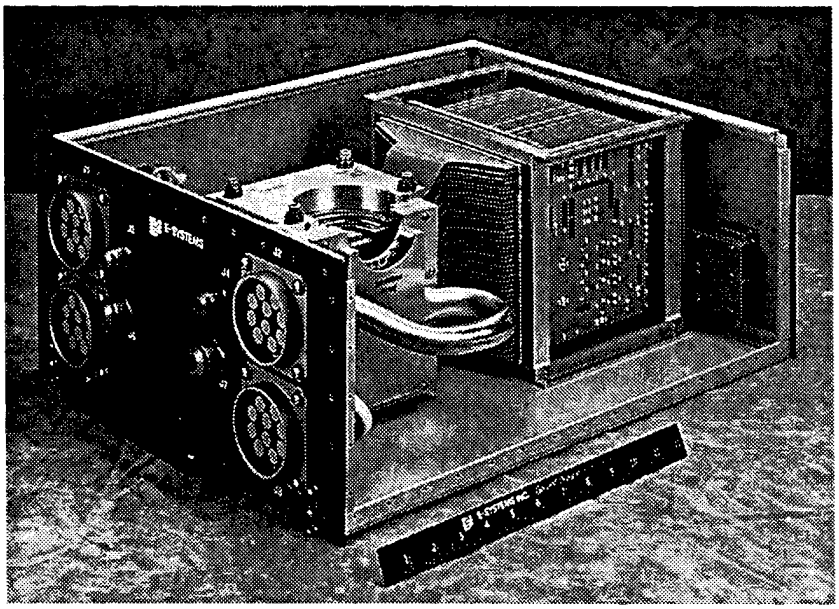


Figure 3-1. 3-D Cube ATR Chassis Model

4. ACCOMPLISHMENTS

During this undertaking of the 3-D Diamond Technology Development Program, significant progress was made toward designing and fabricating substrates, components, tooling, and fixtures for the construction and testing of both 2-D and 3-D demonstration test vehicles. These technology demonstrations/evaluations included 2-D and 3-D diamond MCMs as well as diamond laminate/PCB brassboards. A significant number of these accomplishments are industry "firsts". These leading edge technology accomplishments are summarized below:

1. A total of 30 CVD large scale diamond wafers (3, 4, and 5-inch diameters) were successfully deposited and delivered for this program (0.5 – 1.0 millimeter thickness) with Thermal Conductivity exceeding 1,100 Watts/m°C.
2. 4-inch diameter diamond wafers have been successfully polished to a surface roughness of 0.3 microns.
3. 1-millimeter thick diamond substrates have been successfully laser drilled with over 5,000 high quality via holes (4-mil diameter with a 20-mil pitch).
4. Metallization of large-scale diamond substrates using sputtered Cr-Cu have been successfully developed and process verified.
5. A multi-level metal (Cu/Ni/Ag) sputter/plating sequence has been successfully demonstrated and process verified for the thru-hole via metallization process on freestanding diamond wafers.
6. Double-sided thin-film chip-to-chip High Density Interconnect (HDI) utilizing a metal-dielectric process has been successfully applied to large-scale diamond substrates.
7. Large area polymide ablations utilizing a CO_2 laser has been successfully incorporated as part of the thin-film HDI process on diamond MCMs.
8. Design and fabrication of fuzz button retainer boards for z-axis interconnections between MCMs were successfully completed (incorporates array of 2712 fuzz button contacts located on a 40-mil pitch).
9. A ten-layer stripline rigid/flex circuit board was successfully developed to provide over 190 controlled impedance connections for I/O signal communications to each MCM.
10. A free standing diamond wafer (1-inch square, 1-millimeter thick) has been successfully laminated to a PCB with anisotropic adhesive.
11. A board edge impingement Spray-cooler Atomizer has been successfully fabricated and tested for thermal management of a 3-D stack of diamond MCMs.
12. A copper cooling manifold has been successfully vapor-phase soldered to a metallized diamond substrate edge (diamond laminate/PCB application).

A summary of the other key accomplishments made by program subcontractors and Raytheon during the performance of this contract is provided below:

- Field solver Signal Integrity Models have been completed to address both 2-D and 3-D signal propagation effects through diamond MCMs.
- Computerized Thermal Conduction Models for both laminate and additive diamond MCMs have been completed.
- First silicon of VLSI Special Test Die (i.e., Test Characterization die and Clock Chip) was received and functionally verified by test.
- Fabrication and assembly of a 3-D Diamond MCM Demonstration Test Bed has been completed and integrated into a series of test racks.
- Development of data acquisition/test/measurement software for the 3-D Diamond MCM Demonstration Test Bed has been completed.
- Formal mechanical, thermal, and signal integrity testing of the 3-D Diamond MCM Demonstration Test Bed has been completed.
- Formal demonstration of the 3-D MCM Diamond Test Bed to key Government participants was performed.
- A trade-off study defining the size, weight, and performance advantageous of utilizing 3-D MCM technology in Airborne Military Processors has been completed.
- A non-functional mechanical mock-up of an airborne military processor incorporating 3-D Diamond MCM technology was built and displayed to key senior military planners.

The significance of these accomplishments is many. The diamond laminate/PCB technology offers reduced thermal management system costs in high performance PCB-based computer systems. This reduction is gained by reducing or minimizing cooling fluid rates in PCB-based computers that utilize forced liquid convection cooling techniques over the active chip area. Diamond allows higher heat removal or extraction by the fluid in the same or smaller volume, which translates to significantly lower liquid flow rates for each involved computer system.

Impingement spray cooling technology holds significant promise to erase thermal barriers currently limiting high performance MCM applications and systems. Spray cooling can achieve heat transfer coefficients two orders of magnitude greater than the forced-air convection used in most office computer equipment. It is even an order of magnitude better than the forced liquid convection technique employed in more sophisticated electronics. Up to 500 watts dissipation per MCM can be achieved utilizing lateral thermal conduction alone. This improved efficiency translates into several system benefits including smaller and lighter coolers, less pumping power, and ambient heat exchangers.

The area array z-axis interconnects eliminate restrictions of board edge connector pins, and allow a very large quantity of chips to be interconnected within 1 nsec latency delay time. The interposer technology developed under this program provides for simple, de-mountable methods for z-axis interconnects.

4.1 PACKAGING MILESTONES

A summary of the basic 3-D packaging milestones achieved by this program is shown in Table 4-1. 3-D Diamond MCMs is an enabling technology to support chip-to-chip and module-to-module high-density connectivity and thermal management. The extremely high conductivity of diamond, coupled with electrically insulating nature, makes it an ideal choice for solving 3-D packaging problems. The thermal conductivity is so high as to allow over 80 W/in^3 of power dissipation to be extracted from a stack of diamond substrates by lateral thermal conduction techniques alone.

What the diamond does is laterally conduct the heat generated by the logic out of the "battle zone" of the actively populated cube itself. This frees the designer to fully utilize all of the space between boards to implement a high area density array of vertical interconnects between all adjacent boards in the stack to minimize interconnect delays. Because there is no need to co-utilize this inter-board space to meet cooling requirements, the designer can make use of the most reliable, simple, cost effective, de-mountable, etc., vertical interconnect methods available.

All of these individual accomplishments have led to the fabrication, assembly and integration of a 3-D Diamond MCM Demonstration Test Bed. This test bed serves as a tool for testing and demonstrating the effectiveness of this developed technology. The successful culmination of this program is shown in Figure 4-1 as a pictorial view of the completed test bed hardware.

4.2 DISSAPOINTMENTS

There was only one goal that this program did not achieve. Signal integrity measurements and evaluations up and down through the z-axis structure of the Cube Assembly were not conducted, and therefore could not be compared against the theoretical assessments discussed in Section 9.0. Evaluations such as noise margin, crosstalk, and other signal propagation assessments between adjacent z-axis signal paths had to be abandoned.

This signal integrity shortcoming was caused by the fact that a limited number of interconnect nets associated with each MCM were "open" (i.e., >50 Ω) as determined by probe testing. In particular, some of these open nets were associated with the distribution of the clock signal associated with the "tz" chip on the diamond MCMs. Without this clock signal, it was impossible to propagate the proper pattern of test digital signals to verify active signal interfacing through the 3-D stack. Several signal paths were designed through the stack to provide various crosstalk environments. These paths could not be activated without valid clock distribution.

The cause of these open nets has not been determined. Surface and cross-sectional observations of these diamond MCMs all appear normal with no indications of any issues which would act to compromise the integrity of the interconnect assembly. The mechanical structure of the components involved in the 3-D stack was very robust. Even after several disassembles and reassemble, the continuity through the 5000 vertical paths of the MCMs, rigid/flex circuit, and fuzz button retainer boards remained intact.

These involved MCMs do exhibit partial functionality, and were utilized for a very limited set of passive signal integrity testing. Full thermal testing of the Cube Assembly was conducted, however, and these results are discussed in Section 10.0.

Table 4-1. 3-D Packaging Milestones

Packaging Parameter	3-D Demonstration/Test Vehicle
Packaging Architecture:	Large Scale Diamond MCMs with Area Array Space Boards for Z-Interconnects
Number of MCMs per 3-D Stack:	3 Boards Test/40 Board Target System
MCM Board Size (Active Area):	3" x 3"
Power Dissipation per MCM:	83 W to > 1 KW (Variable)
Chip Size/I/O Count/Power:	Test Die: 10mm x 10mm/400 Pads Variable Power: 19W to 150W/Die
Clock Rate:	Variable to > 500 MHz Interconnect Design to > 2 GHz
Through VIAs per MCM:	5400 to 7300 (Solid Filled VIAs)
"Fuzz Button" Z-Interconnects:	2000/Board; 5000 to 10,000 for Target System
Number of MCM Metal Layers:	5 Layers Top/8 Layers Bottom (HDI)
Thermal Management Technique:	Board-Edge Spray Cooler
System Volume (with Cooler):	0.02 ft^3 test/0.12 ft^3 for 40 Board Target System
Power Density:	>80 W/in^3

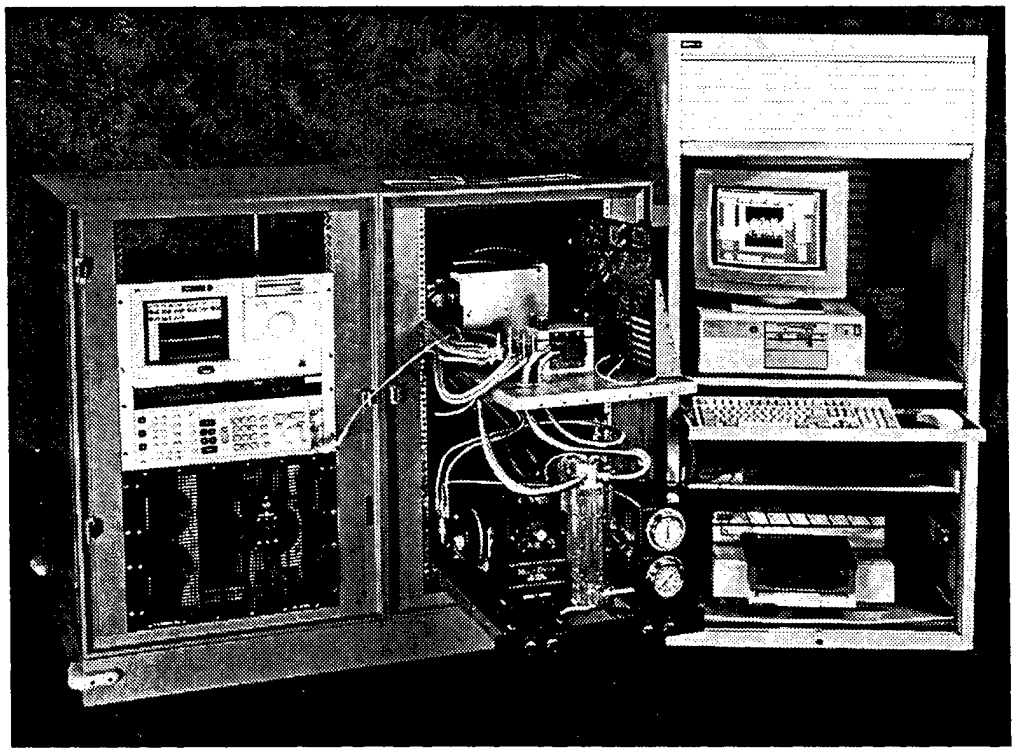


Figure 4-1. 3-D Diamond MCM Demonstration Test Bed

5. 3-D PACKAGING DESIGN

Figure 5-1 provides an exploded view of the 3-D Diamond MCM Cube Assembly. The 3-D stack consists of 3 diamond MCMs, 8 Fuzz Button retainer boards, Top and Bottom Turn-Around boards, 3 rigid/flex circuits, and a clamping fixture that compresses and holds the stack under pressure. The 3 diamond MCMs are stacked one on top of the other. Between each MCM is a compression-contact interposer (Fuzz Button retainer board) which provides connections face-to-face between adjacent MCMs. Serpentine routing through the 3-D stack emulates a total 40 MCM stack. The top and bottom turn-around boards take signals routed out of the stack and turn them back into the stack to enable this serpentine routing.

Figure 5-2 provides a conceptual illustration of the final MCM stack configuration in the holding fixture. Notice that three diamond MCMs are involved in this stack. These elements are discussed in the following sections.

5.1 MCMs

The MCM design is the focal point of these 3-D technologies. It contains the diamond substrate with cooling fins to interface to the spray-cooler, the test characterization die or ICs, and the thin-film interconnect between the die.

The diamond MCM is double-sided with five High-Density Interconnect (HDI) layers on the component side and eight HDI layers on the interconnect side. Figure 5-3 provides a layout profile for the diamond MCMs.

All three MCMs in the Cube Assembly are the same design. The component-side contains nine total die. Eight of these die or ICs are called Test Characterization die ("ti" die) and contain the controllable heater and signal sources. The center die ("tz" die) is a Clock Chip and distributes clock to the eight "ti" chips. The "ti" die is a voltage controlled current source capable of dissipating up to 150 watts per chip. With all chips fully powered, dissipations greater than 400 watts per MCM were possible. Based on this, the design goal of 500 watts per MCM was chosen to size the power delivery system to the 3-D cube assembly.

This "ti" die also has on-chip circuitry for pattern generation and data collection functions that support signal integrity evaluations. The "Heater" and "Signal" terminology originate from an early assumption that the "ti" die would not function both as a heater and a signal generator simultaneously. Therefore, the chips were divided into these two groups. However, the "ti" chips were built to provide signal generation even when the chip is performing a "Heater" function. The resulting configuration was retained because of its redundancy benefits. The two loops are identical and provide a graceful degradation of test capabilities should failures occur.

- Number of Diamond MCMs: 4
- MCM Size: 7.5 cm x 7.5 cm
- Max Power Per MCM: 500 Watts
- Clock Rate: 500 MHz
- Number of Interlayer Connections: 2712
- Number of External Connections: 660
- Power Density: >80 W/in^3

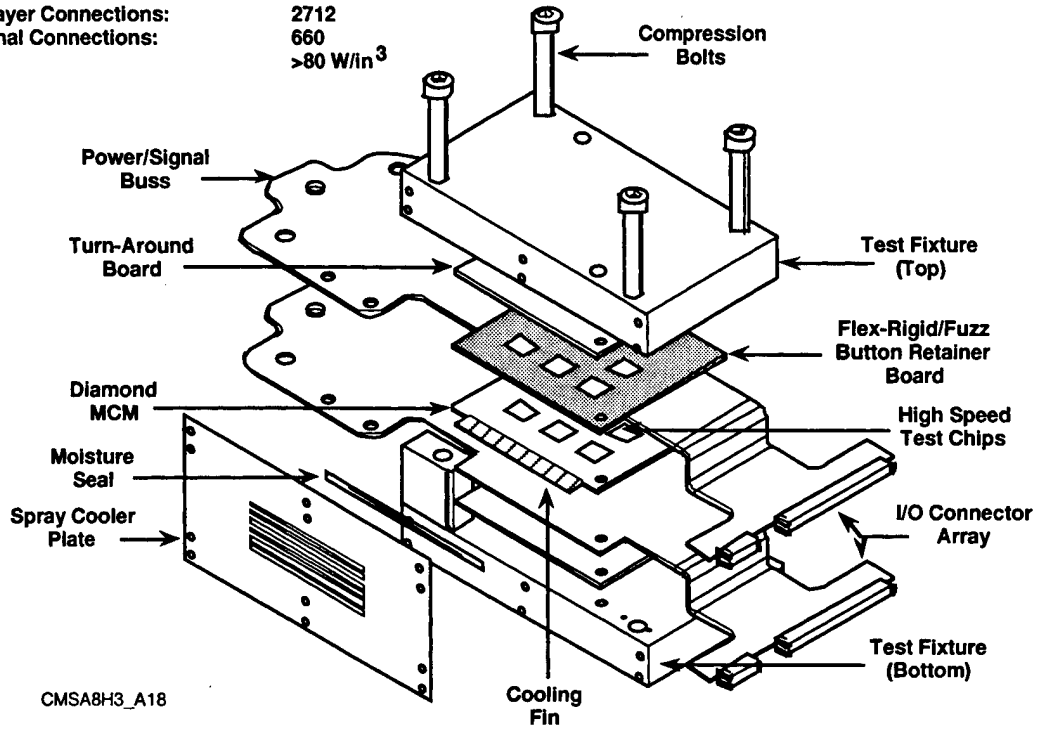


Figure 5-1. 3-D Diamond Cube Assembly

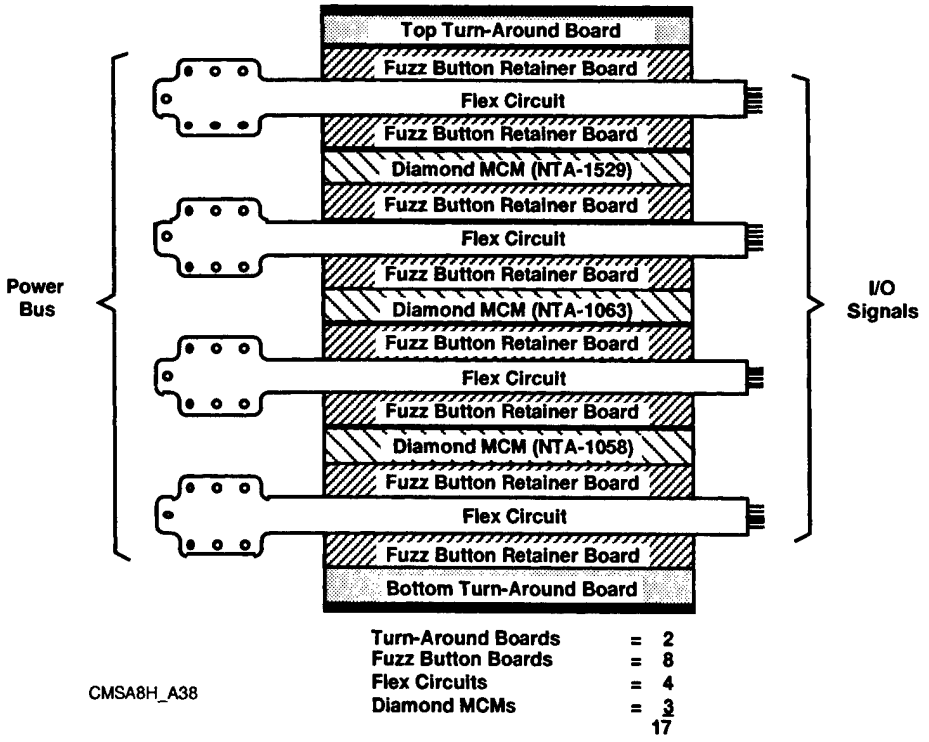


Figure 5-2. Illustration of 3-D MCM Stack

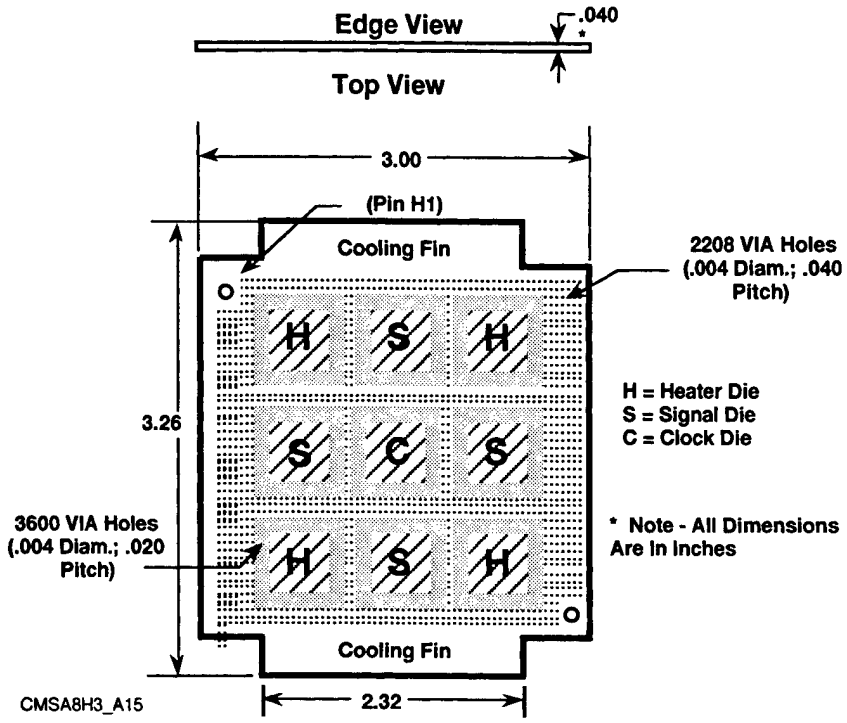


Figure 5-3. Diamond MCM Layout Profile

Areas of the HDI layers on the component-side are ablated away to allow the die to be directly attached to the diamond surface. These 400 x 400-mil die are mounted directly to the diamond with 2-3 mil of thermally conductive epoxy. After die attach, the die pads are wire bonded to an array of pads that encircle each die.

5.2 RIGID/FLEX CIRCUIT

Methods of implementing, conveniently and practically, high-density arrays of vertical interconnects between adjacent MCMs must satisfy several needs simultaneously. Since the interconnects must support high performance MCMs operating at clock rates in excess of 250 MHz, the 3-D interconnect structure must guarantee that signals are propagated with minimum levels of distortion. Therefore, controlled impedance signal paths must be treated as a transmission line, characterized by impedance, loss, and electrical length.

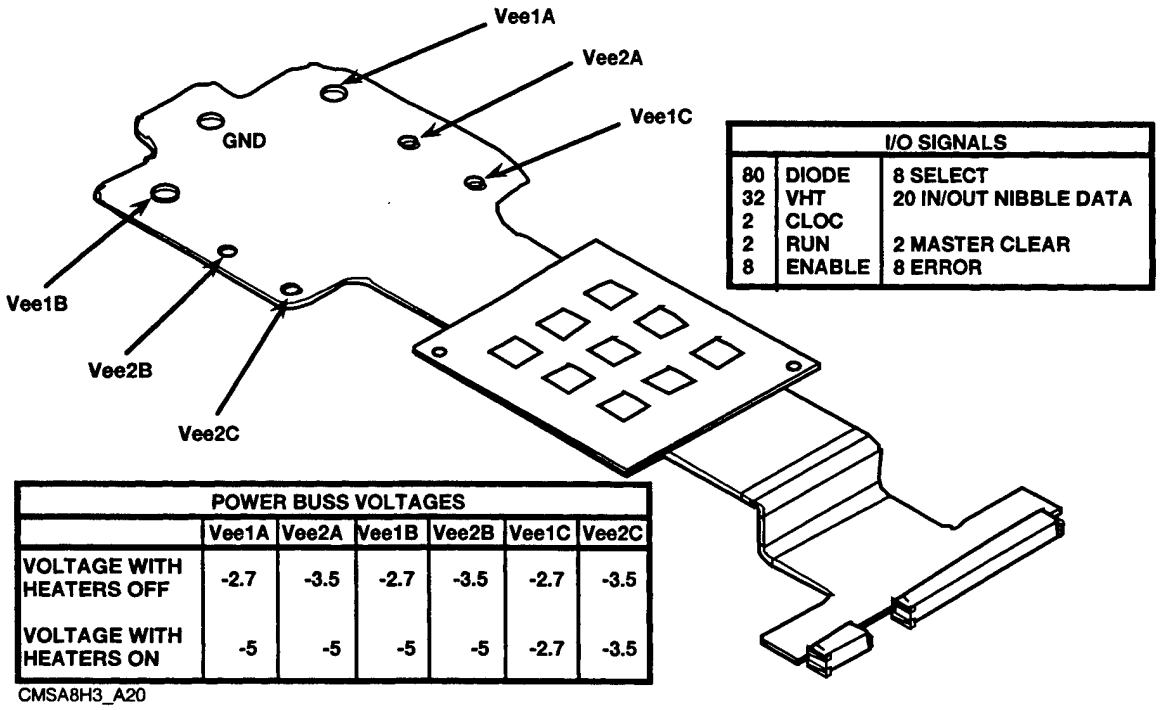
The vertical interconnect structure must allow for a simple, de-mountable technique for MCM replacement in the event of a failure. The 3-D structure must also be relatively thin, to allow a large quantity of MCMs to be stacked while keeping the vertical signal path as short as possible.

Finally, there is the need to supply external signals and power to each MCM in the stack. Therefore, the 3-D structure must be provided with a large quantity of controlled impedance I/O connections for signal communications to and from the outside world, plus power supply mounts for high current input to the chips mounted on the MCMs.

After evaluating several concepts, a rigid/flex circuit or board technique was selected. The flexibility and impedance requirements dictated that a controlled impedance rigid/flex circuit must be used, and is illustrated in Figure 5-4. The flexible area of the board provides the needed fan-out

to mate with the Test I/O Board. 190 I/O signal paths were required to control and communicate with each MCM. A 10 layer stack-up (8 internal layers and 2 external pad layers) for this rigid/flex circuit was designed utilizing stripline for the controlled impedance signals. The controlled impedance lines carry the signals from the controlled impedance connector to the center area of the board where connection to the MCM occurs. Mictor™ controlled impedance connectors were utilized to provide 190 signal I/O per rigid/flex printed wiring board. The design fabrication drawing for this rigid/flex circuit is shown in Figure 5-5.

High current power and high-speed signals are delivered to the 3-D stack via these flexible wiring boards. Six voltages are input to the 3-D stack via the rigid/flex printed wiring boards. Eight, 1 ounce copper, plane layers are used to handle the 100 amps of current required by two of these voltages. The power cables are connected directly to the printed wiring boards with a bolted compression connection. There is a mounting hole for each filled copper area.



I/O SIGNALS		
80	DIODE	8 SELECT
32	VHT	20 IN/OUT NIBBLE DATA
2	CLOC	
2	RUN	2 MASTER CLEAR
8	ENABLE	8 ERROR

POWER BUSS VOLTAGES						
	Vee1A	Vee2A	Vee1B	Vee2B	Vee1C	Vee2C
VOLTAGE WITH HEATERS OFF	-2.7	-3.5	-2.7	-3.5	-2.7	-3.5
VOLTAGE WITH HEATERS ON	-5	-5	-5	-5	-2.7	-3.5

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Figure 5-4. Design Concept for Rigid/Flex Circuit Board.

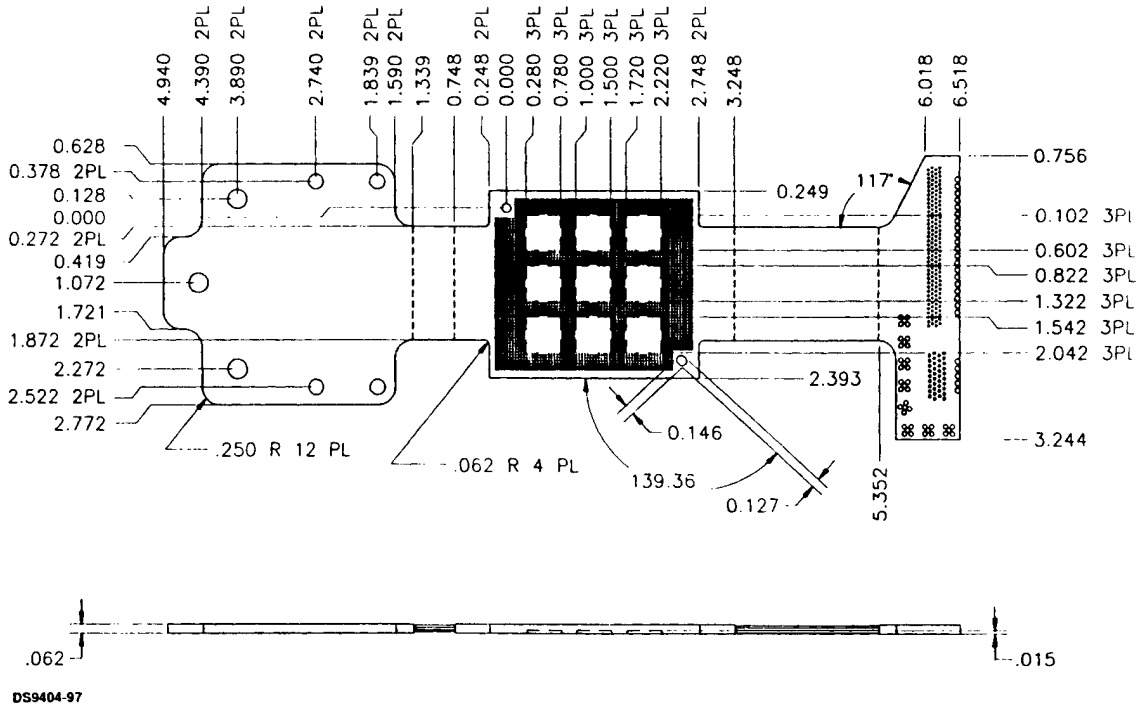

Figure 5-5. Rigid/Flex Fabrication Drawing

Power cables from the 3-D Diamond MCM Test Bed power supply are bolted to the mounting holes in the rigid/flex circuitry that extends from the 3-D stack. The power bus bars of the Turn-Around boards are also connected to the power cable connection points. The six voltages supplied by the power supply are listed below:

VEE1A	-2.7V
VEE2A	-3.5V
VEE1B	-2.7V
VEE2B	-3.5V
VEE1C	-2.7V
VEE2C	-3.5V

The test characterization die associated with each MCM receives its power from the fuzz button connections of the Fuzz Button Retainer Board that is stacked above and below the rigid/flex circuit. The Fuzz Button board provides power supply input connections and distributes the power to the MCM via the fuzz button array.

These voltages support three separate power zones in the 3-D stack. The eight "ti" chips on each MCM are divided into two separate power zones. VEE1A & VEE2A power the four "ti" chips placed in the corners of the nine die arrangement of the MCM (i.e., corner die loop). VEE1B & VEE2B power the four "ti" chips placed in between the corner die on the perimeter of the nine die arrangement of the MCM (i.e., edge die loop). The center chip in the nine die arrangement (the "tz" or clock chip) is powered via the VEE1C & VEE2C power zones.

5.3 Fuzz Button Retainer Boards

The Fuzz Button Retainer Boards provide z-axis electrical interconnections between the MCMs. Figure 5-6 shows the cross-section of these retainer boards sandwiched in between two diamond substrate MCMs. The center rigid area contains the two fuzz button array connectors (one on top and the other on bottom) of the rigid/flex circuit previously discussed.

Figure 5-7 is a picture of the initial artwork for the Fuzz Button Retainer Boards. The rigid center is where the fuzz button arrays are mounted. The squares on the drawing are indentations or cutouts to provide necessary clearance for the ICs when the MCMs and retainer boards are stacked together.

Fuzz buttons are randomly interwoven gold wire formed into small cylinders. These cylinders are inserted into non-plated through-hole vias in the retainer board on a 40-mil grid to match the landing pads on the diamond MCMs. A bevel at the base of the via in the retainer board is required to provide a retention feature for the fuzz button. When buttons are compressed in the final assembly step, the compression force causes the button to spread out at the bottom of the via into the beveled area.

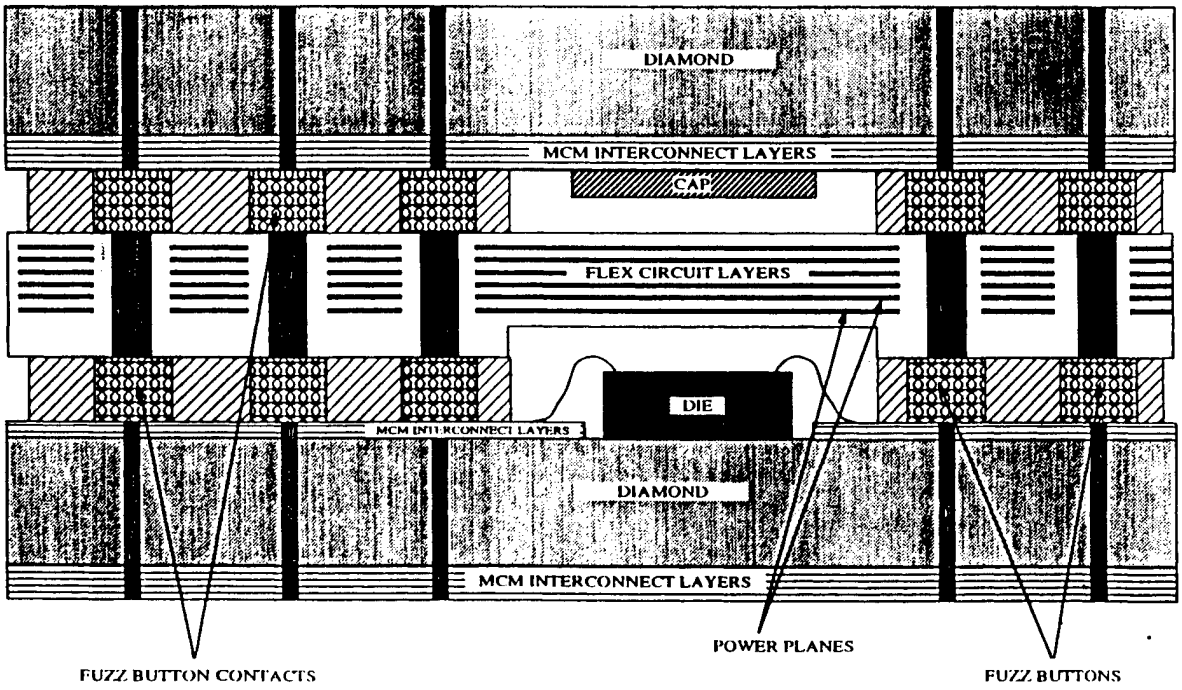

Figure 5-6. Cross-Sectional of 3-D Diamond Cube Stack

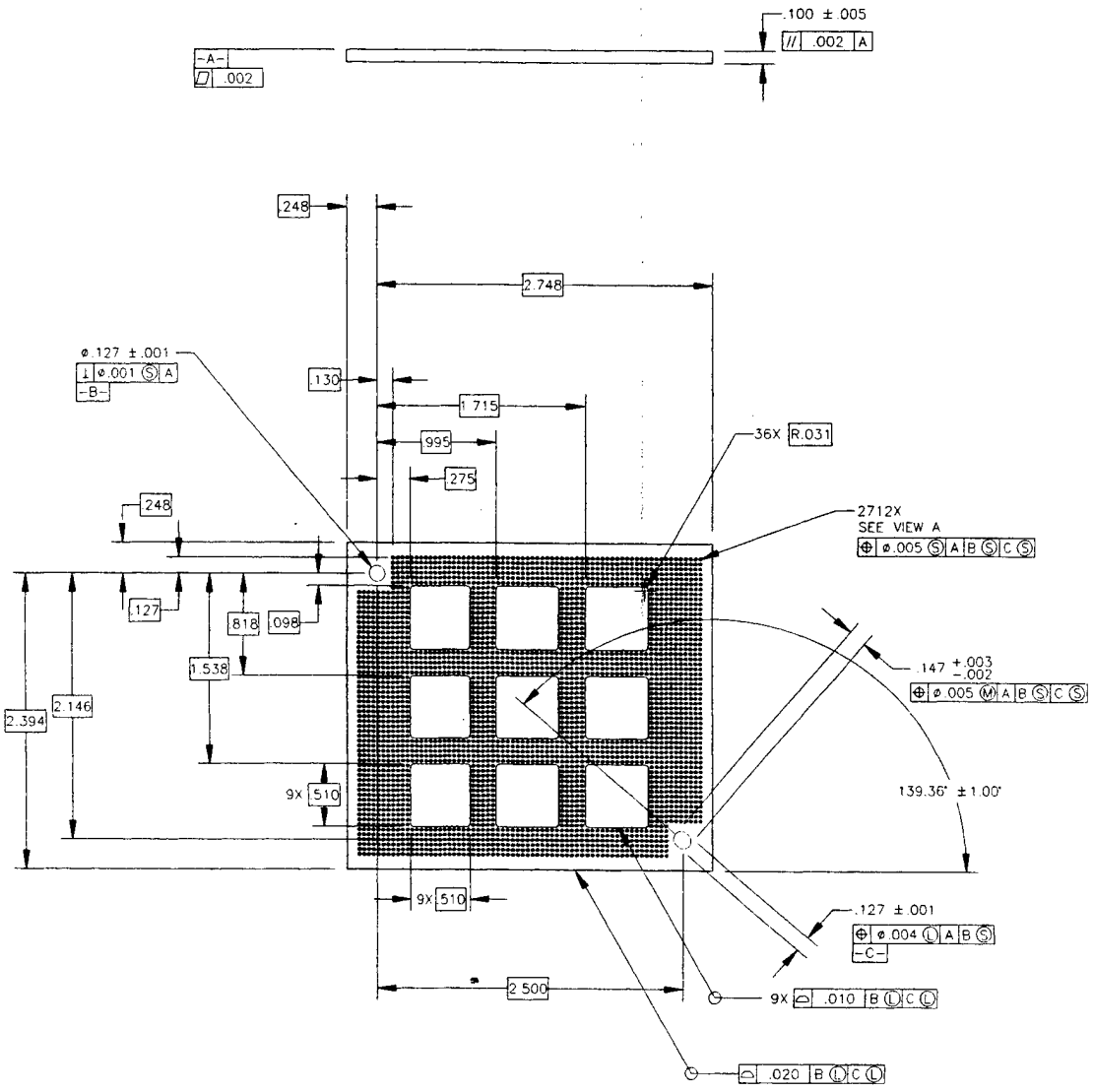

Figure 5-7. Fuzz Button Retainer Board Design Artwork

After the retainer boards and the rigid/flex circuit are assembled in the 3-D stack between adjacent MCMs, the clamping fixture compresses the stack together. When compressed, the fuzz buttons make contact to the landing pads on each MCM. It transfers the signal through the fuzz button to the via-structure in the rigid/flex circuit. The via connects the signal to the appropriate routing layer for transmission to/from the external interfaces, such as the Test I/O Board and the power inputs; or it connects to a via that passes the signal straight through to the next MCM in the stack.

5.4 Top & Bottom Turn-Around Boards

The Turn-Around Boards are positioned at the top and bottom of the 3-D MCM Stack. Signals routed out of the 3-D stack from either the top of the bottom are "turned-around" and routed back into the stack by the turn-around boards. This provides a much longer signal path through the 3-D structure, thus emulating 3-D stacks greater than 3 MCMs. The extra copper layers in the turn-around boards supplement the power distribution across the cube, thereby reducing the resistance for power distribution across the cube. Even with these extra power layers, the single-sided power distribution of the 3-D stack has the potential to create a significant voltage drop across the substrate. Therefore, external power bus bars were added to provide a solid copper path from one side of the turn-around boards to the other. This supplemental approach will minimize the voltage drop across the substrate by providing a lower resistance path to the other side. Figure 5-8 shows a top view of the design artwork for a turn-around board. The tabs on the left and right extend outside the clamping fixture and are used to jumper the power to the other side of the cube. The power bus bars are soldered to the pads on the extended tabs in order to provide connection to the internal layers of the turn-around boards.

5.6 Clamping fixture

The clamping fixture associated with the 3-D Diamond MCM Cube assembly performs three functions. The first function is to accurately align all the components (MCMs, Fuzz Button boards, and turn-around boards) in the stack. The second function is to compress the Fuzz Button contacts sufficiently to provide an electrically conductive signal path through the stack. The third function of the holding fixture is to provide a mounting interface for the spray-cooler heads.

The fuzz button contact relies on compressive force to make the electrical connection between the MCM, the fuzz button boards and the turn-around boards. The fuzz button is fabricated from beryllium copper wire which gives the button its spring characteristics. The spring constant is a factor of the wire diameter, temper, and the density of the button. The button used on this program was designed to compress .010 inch with a nominal force of 3 ounces. The fuzz button board contains 2712 buttons per side; therefore, a clamping force of 510 pounds is required to fully compress the fuzz buttons. The fixture is required to accurately impart this force and then maintain the force while the cube is subjected to temperature cycling. These requirements necessitated the addition of a compliant actuation mechanism. The mechanism chosen was a belleville spring stack. Employing a stack of belleville springs on the clamping

bolts increases the number of bolt rotations required to achieve a given force; therefore, reducing the force per turn ratio. This allows for a finer adjustment of the compression force.

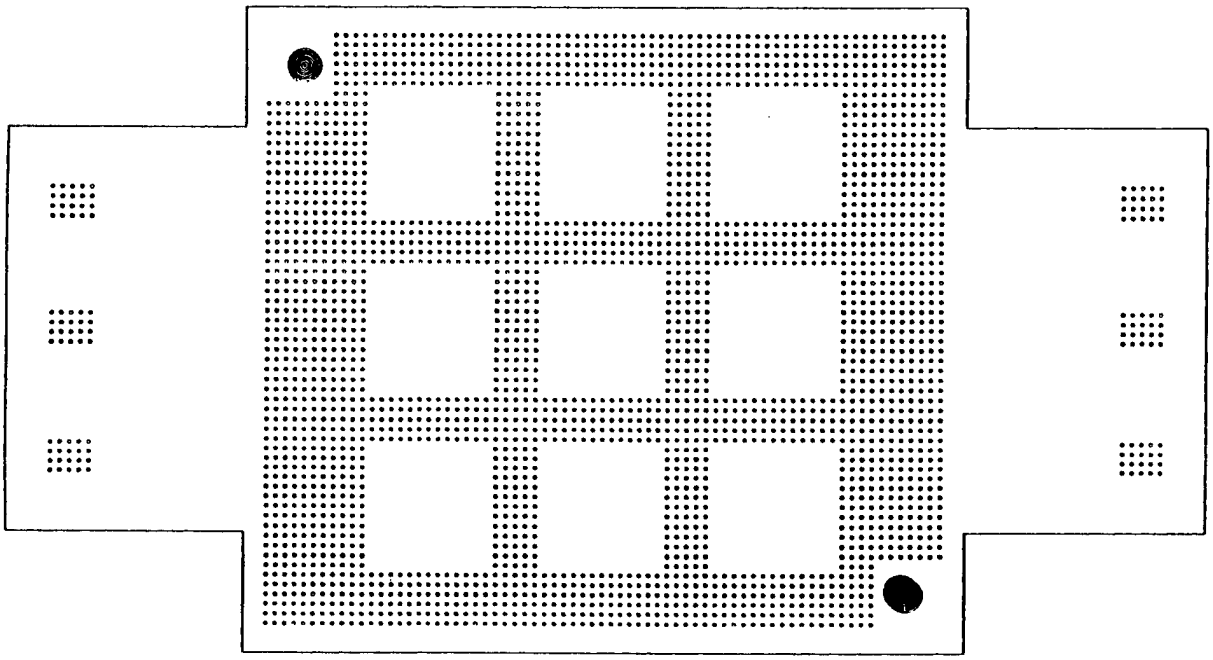

Figure 5-8. Turn-Around Board; Top View

The clamping fixture consists of a base, a platen, a spacer and four mounting bolts with belleville spring washer stacks to cushion the bolt-to-platen interface. The clamping fixture also supports the mounting of the two spray cooling nozzle arrays to facilitate the cooling of each MCMs diamond fins that protrude into the cooling chamber on each side of the clamping fixture. Figure 5-9 provides a perspective design drawing for this clamping fixture.

Alignment of the MCMs, turn-around boards and the fuzz button retainer boards requires precision and flexibility. The clamping fixture must precisely locate the components but not cause them to be stressed during temperature cycling. The alignment of the MCMs and the Fuzz Button boards is accomplished using a two-pin design located at opposite corners of the clamping fixture. The MCMs, turn-around boards, and the fuzz button boards all have a complementary hole and slot pattern. The hole in each of the mating parts is only large enough to clear the pin. The hole locates the mating parts in both the X and Y directions but does not control rotation. The slot controls rotation while allowing for tolerance build up between the pins and relative motion between the fixture and the components due to CTE mismatch . The worse case tolerance build up between the mating parts is 16 mils diameter. Since the contact pads and the fuzz buttons are 20 mils diameter and the contacts are located on a 40 mils pitch, the tolerance allowance ensures contact while disallowing shorting.

5.7 Board Edge Heat Removal

The density of a 3-D stack comprised of closely spaced high-powered MCMs presents a significant challenge to the thermal management system. Once the cube is assembled and all external interfaces connected, only two faces of the cube remain accessible for cooling. Heat must be conducted laterally from the center of the cube to the two faces reserved for cooling. Synthetic diamond substrate material offers the superior thermal conductivity to meet this challenge. Next, heat must be removed from the two faces and expelled from the system through some type of heat exchanger. Spray cooling is exploited to achieve high heat transfer efficiency with minimal hardware overhead for the cooling subsystem.

Heat removal from the face of the cube assembly is achieved through a novel spray cooling technique that exploits the phase-change properties of liquid. The graph in Figure 5-10 compares the heat transfer efficiency of several common-cooling techniques. Spray cooling can achieve a heat transfer coefficient two orders of magnitude greater than the air-forced convection used in most office computer equipment. It is even an order of magnitude better than the liquid-forced convection popular in more sophisticated electronics.

The phase change process is sustained by continuously coating the hot diamond edge surface with a uniform thin film of Flourinert™, the preferred heat transfer fluid. As shown in Figure 5-11, this is accomplished by replenishing the fluid by a fine spray as it evaporates. This mist is created by spray nozzles directed at protruding edges of the diamond MCMs.

The fins of each MCM extend into the spray cooling chamber. The conduction path for the heat is from the die through the diamond substrate to the exposed fin area in the cooling chamber. The substrate edge extends 0.78 cm into the cooling chamber. This provides 9.1 cm^2 of surface area per cooling fin. This surface area is sprayed with an atomized dielectric fluid that evaporates when the droplets contact the surface. This evaporation extracts the heat from the surface and produces the high heat transfer coefficient required to handle the power dissipation of the diamond MCMs. Fluorinert FC-87, manufactured by 3M, is the dielectric fluid used and has a boiling point of 31 °C. This boiling point was selected to ensure that the liquid evaporated on contact since evaporation is critical to the performance of the cooling system.

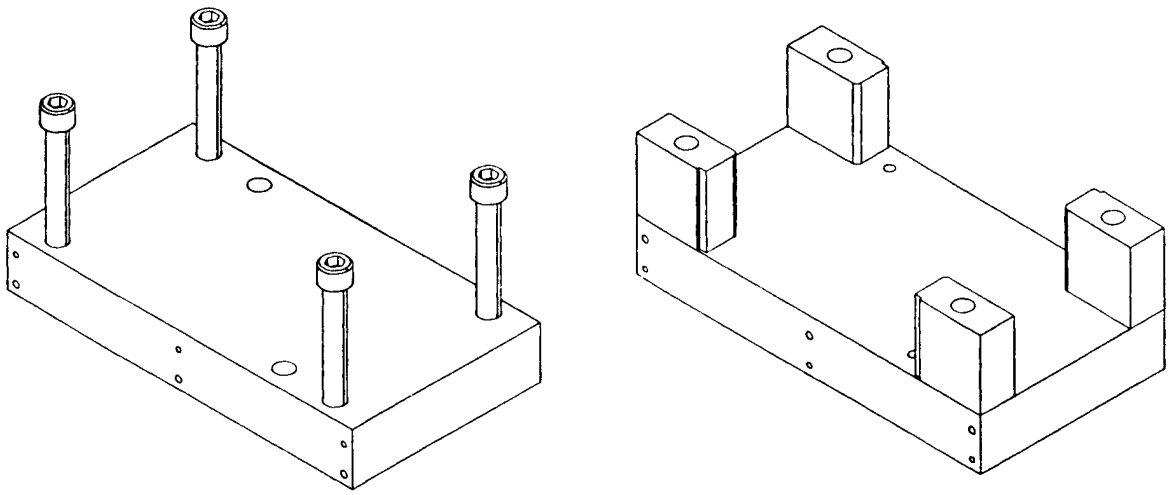

Figure 5-9. Design Drawing for Clamping Fixture

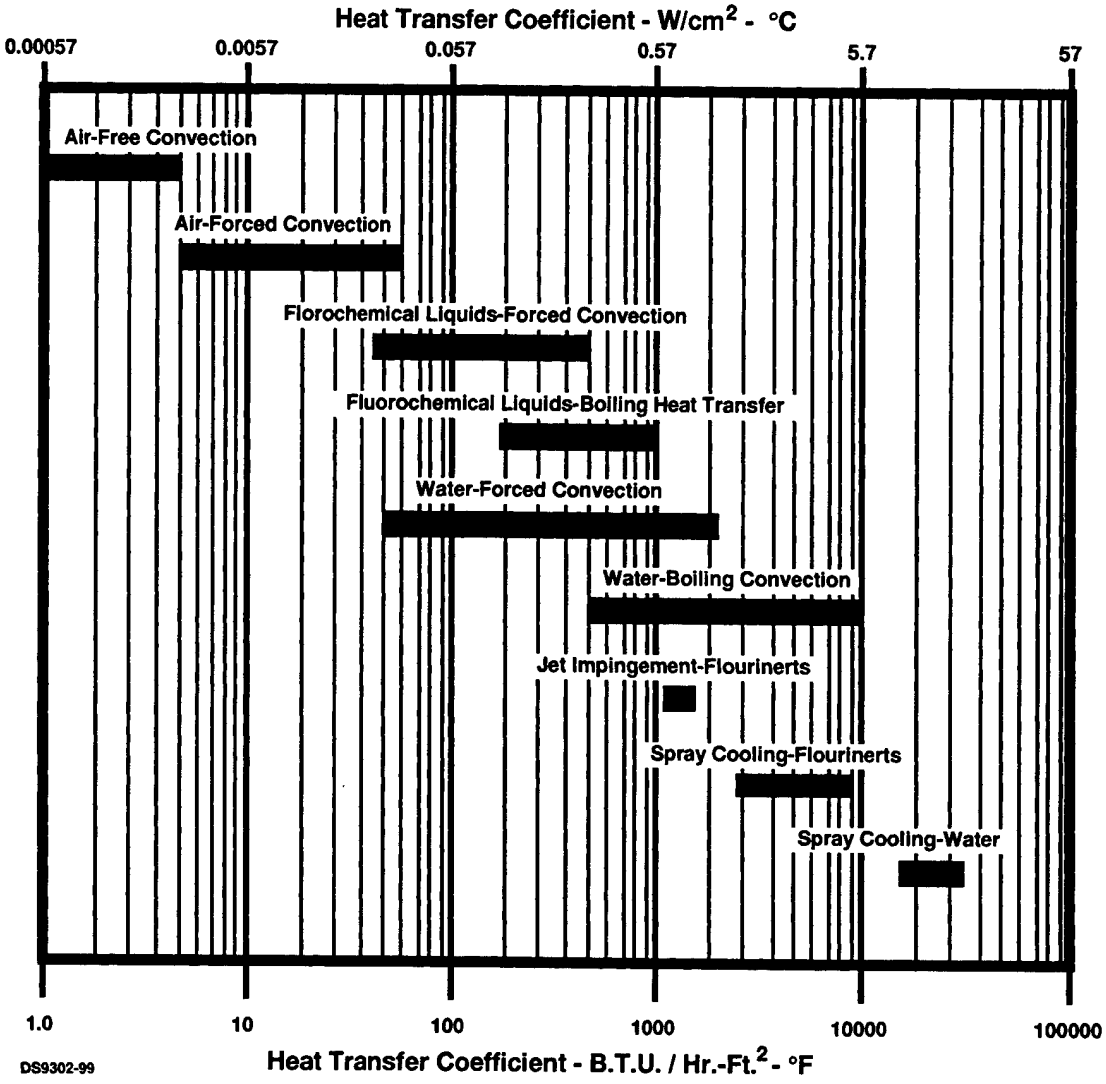

Figure 5-10. Heat Transfer Comparison

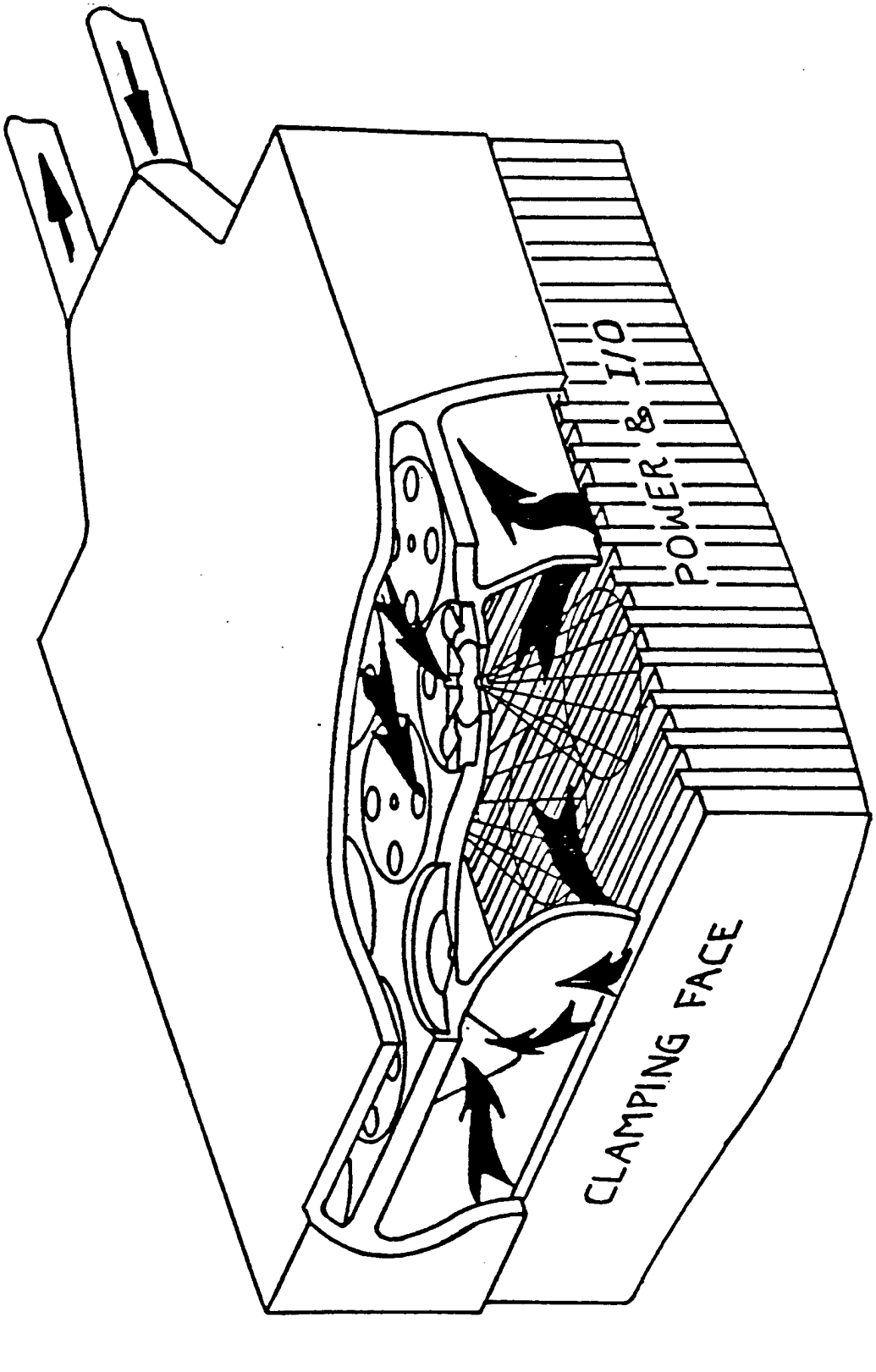

Figure 5-11. Spray Nozzle Concept

6. FABRICATION OF THE 3-D DIAMOND MCM CUBE ASSEMBLY

Figure 6-1 provides a photograph of the completed 3-D Cube Assembly shown in its final hardware configuration. The following sections provide brief descriptions of the fabrication processes and procedures for building this assembly supported by photographs of the final fabricated products.

6.1 Fabrication of Rigid/Flex Circuitry

The construction of the rigid/flex circuit boards had many constraints that significantly increased its fabrication complexity.

1. It required 50 Ω controlled impedance lines for transmission of the 500 MHz clocks and other critical signal paths. Signal risetimes are 200 to 300 picoseconds. Significant care was taken to ensure the signal traces adhered to the 50 Ω requirement.
2. The 10-layer stackup was required due to the signal density at the Test I/O Backplane interface, spacing requirements to maintain impedance, copper required to support power distribution, and the 0.040" grid spacing of the fuzz button arrays.
3. The fuzz buttons in the fuzz button arrays are placed on a 0.040" grid and each button in the grid requires a via in the flex circuitry. The "picket fence" caused by the 0.040" grid via pattern significantly reduces the amount of copper available for power distribution. To maximize available copper, via sizes and clearances were minimized.
4. The 10-layer stackup and impedance requirements for the flex circuit drove the thickness of the assembly. A thicker assembly would allow the reference planes to be farther apart thus allowing larger trace widths increasing producibility. However, producibility of the vias would be adversely effected due to the increase aspect ratio between via depth and via diameter.
5. The 10-layer stackup also presented problems for the controlled impedance requirements. The flex circuit is required to be flexible in the region between the stack and the I/O connectors to support connection to the Test I/O Backplane. The more layers laminated together, the more rigid the assembly becomes. Therefore, a minimum number of layers should be laminated together in the regions required to be flexible.
6. A layer of epoxy glass is laminated to both the top and bottom of the rigid area to insure assembly integrity of the connectors.

A picture of the final fabricated rigid/flex circuit is shown in Figure 6-2. Displayed on the right side of this figure are two MICTOR connectors (one 38-pin and one 152-pin) that provide external connections to the Test I/O Board. MICTOR connectors are 50 Ω controlled impedance connectors from AMP CORP., which provide impedance matched connections for high-speed signals. The 38-pin connector provides connection for the two nibble data buses that operate at 500 MHz clock rates and other edge sensitive signals. The 152-pin connector is used mainly to provide external access to the total 81 temperature sensing diodes associated with each fully populated diamond MCM.

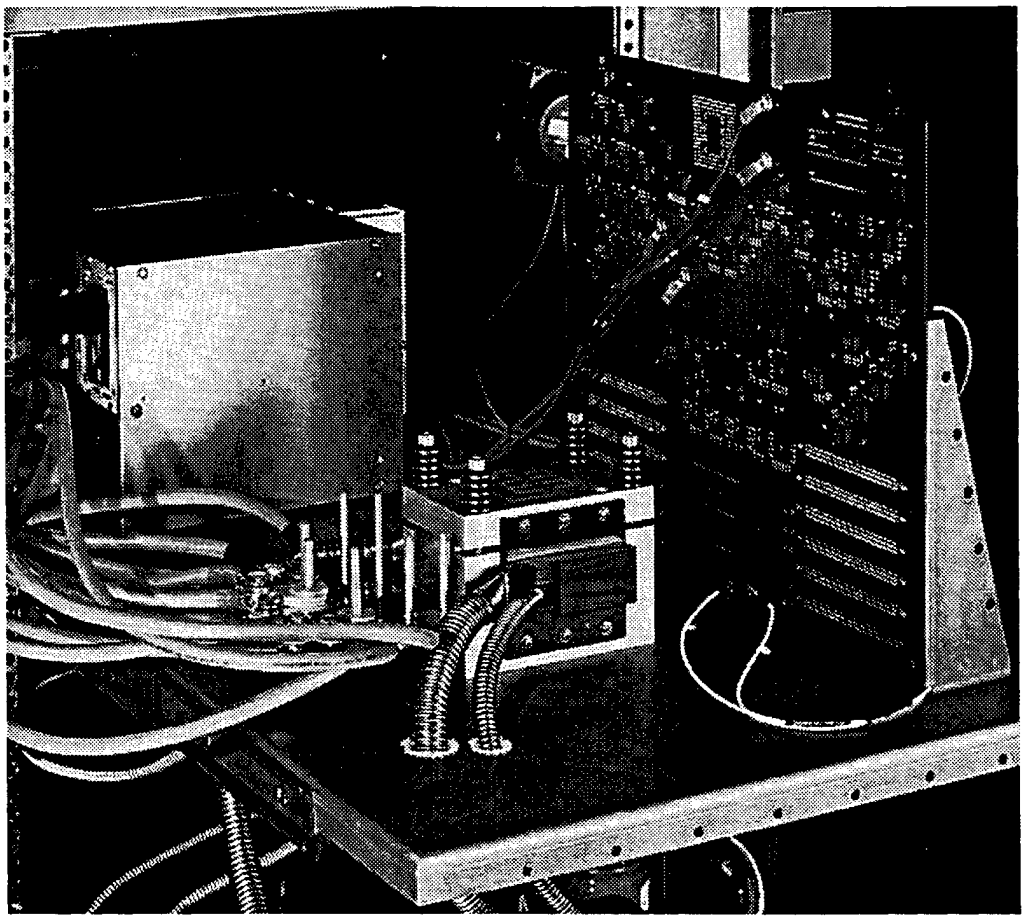

Figure 6-1. 3-D Cube Assembly Shown in Final Hardware Configuration

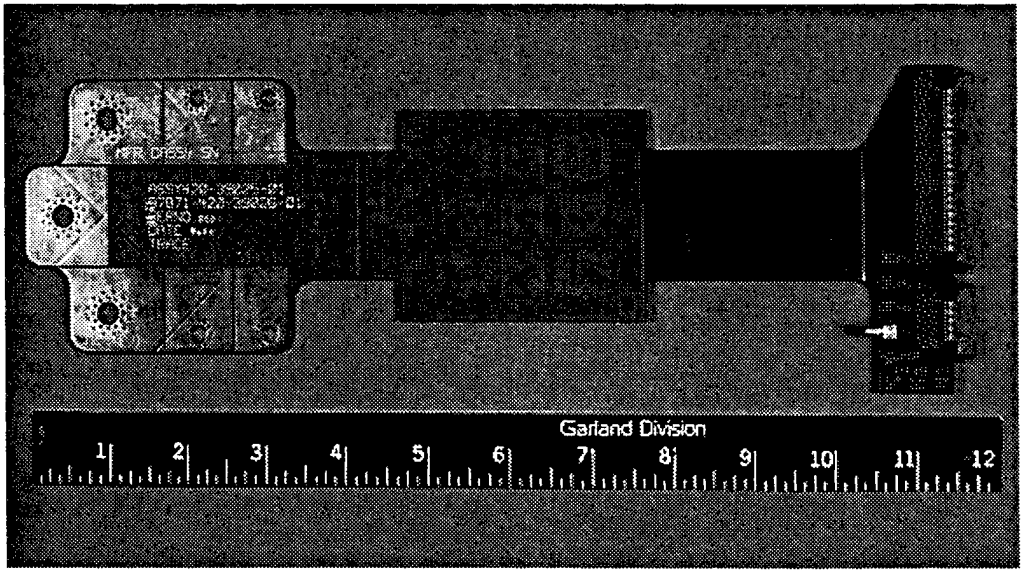

Figure 6-2. Photograph of Completed Rigid/Flex Circuit Board

6.2 Fabrication of Fuzz Button Retainer Board

Precise positioning of the wire button contacts, relative to the MCM and the rigid/flex circuit board contact pads, is critical to the function of the Z-axis interconnect. The function of the fuzz button retainer board is to precisely locate the wire button contacts and retain them to the rigid/flex circuit board.

Wire button contacts or fuzz buttons are made of a single strand of randomly formed gold plated wire, approximately 1-mil in diameter, shaped into a cylindrical "Brillo pad". A low inductance and resistance are the result of randomly connected parallel paths, sometimes referred to as "cancellation effect" [1]. Random contacts under compressive forces give the fuzz button a self cleaning property as well as high current carrying capacity. This form of vertical spacer in a 3-D structure offers flexibility, durability, and reparability by elimination of soldered and wire-bonded contacts.

The retainer board that holds these fuzz buttons is fabricated from 100-mil thick plastic material. The retainer boards have a unique profile that locks the wire button contact into the hole after insertion. The material has 2712 20-mil diameter holes with 25-mil diameter countersinks machined on a 40-mil pitch to correspond to the wire button contact locations. The wire button contact is inserted into the hole and then compressed to fill the countersink on the backside of the retainer board. The expansion into the countersink is what retains the wire button contact on the board. The holes are required to be located within a 4-mil diameter area. The countersink feature requires that conventional CNC machines be used to drill these holes. The material thickness and the hole density presented fixturing problems during the machining operation. The wire button contact supplier utilized a sandwich technique where the retainer material is held between two aluminum plates during the machining operation.

Upon completion of this fabrication process the wire button contacts were inserted into the holes and then compressed to fill the countersink and form a .254 mm (.010 in) tall spherical protrusion. The completed assembly contains 2712 vertical signal paths. A photograph of the completed fuzz button retainer board with all 2712 inserted buttons is shown in Figure 6-3.

6.3 Fabrication of Diamond MCMs

The diamond MCM process development consists of Texas Instruments and GE's High Density Interconnect layers of metallized polyimide on diamond substrates. Raytheon performed the population and wire bonding of integrated circuit chips and capacitors on the resulting diamond substrate/interconnect structures.

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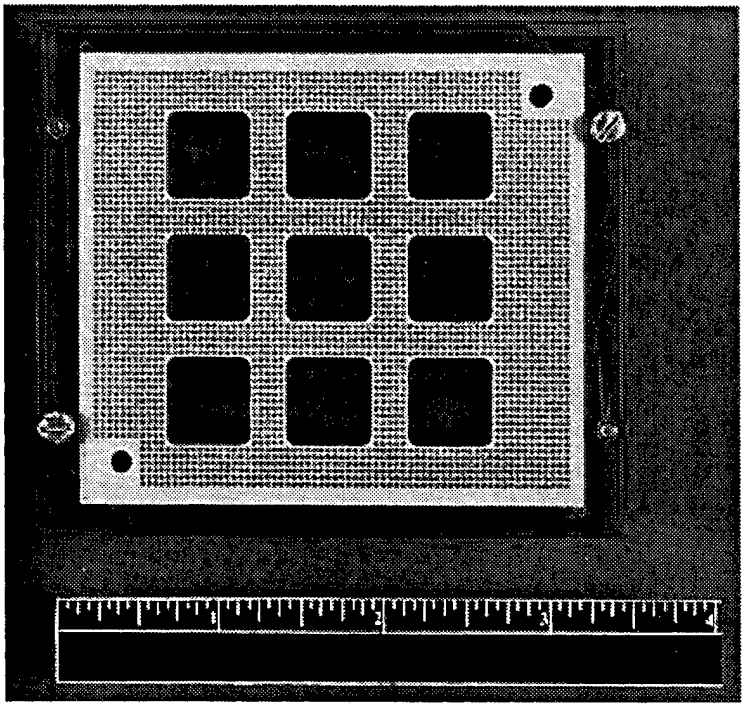
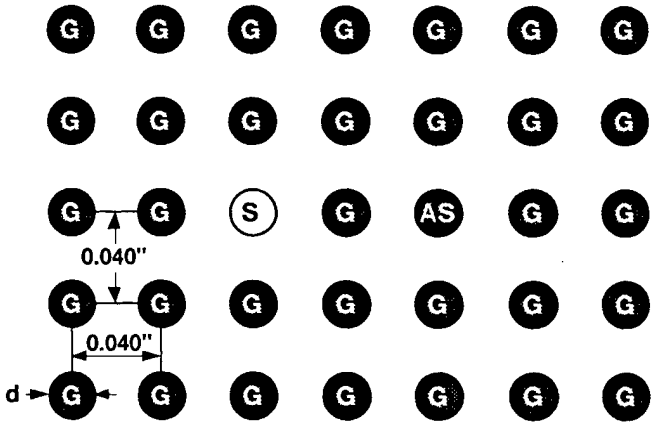
[1] CINCH Connector Division, Elk Grove Village, IL; "Test Report Summary," Report No. CIN: APSE, April 15, 1991



Hardware Implementation



G = Ground
S = Signal
AS = Alternate Signal
d = Cell Diameter

Array of Vertical Cells (Top View)

CMSA8H3_A19

Figure 6-3. Fuzz Button Retainer Board

6.3.1 Metallization of Diamond Substrates

The diamond substrates utilized in this process development were fabricated by Norton Diamond Film, and both sides of the substrates were metallized by Cray Research, Inc., by sputtering chrome and copper and then plating nickel and gold using CAD data developed by Texas Instruments. Table 6-1 provides a listing of all the basic diamond substrate materials provided by Norton Diamond Film over the duration of this program. In all, over 35 large freestanding diamond substrates were deposited and provided by Norton. The total seven 4-inch substrates provided to Raytheon (formerly E-Systems-Garland, or ESY) for their Task 3 activities in support of the fabrication and testing of the 3-D Diamond MCM Demonstration Test Bed is shown in the second to last row of this table.

For detailed descriptions of the substrate metallization process developed by Cray Research, refer to their "3-D Diamond Project Tasks 1A & 1B Final Technical Report, September 20, 1995" listed in Section 2.0. A picture of a successfully metallized diamond substrate is shown in Figure 6-4.

6.3.2 Thin-Film Interconnect Structure

Upon receipt of sample metallized substrates from Cray Research, Texas Instruments performed extensive visual inspections, surface topology measurements, thermal shock using liquid nitrogen, peel tests, wire bond pull tests, and laser drilling directly over microblister sites to determine the compatibility of the metallized substrates to their HDI process. Texas Instruments concluded that Cray's substrate metallization was compatible with the HDI process.

In addition to the examination of compatibility between Cray's substrate metallization and their HDI process, Texas Instruments and GE examined the unique technical issues related to HDI processing on metallized diamond substrates. Those issues included, but were not limited to, thick metallization (37 - 50 μm thick as opposed to the usual 4.5 μm), large area laser ablation of polyimide layers, double-sided design issues involving fixturing and processing, process characterization and testing for high speed applications, and rework capability. For a detailed description of the general methodology, the technical issues, and the conclusions reached by Texas Instruments as a result of their efforts, refer to their "3-D Diamond Project Task 1B Final Report, August 10, 1994" listed in the in Section 2.0.

In TI's HDI process, 4 μm thick copper is the standard layer metallization thickness and is referred to as a thin metal layer. A thick metal layer refers to 37 - 50 μm thick copper, otherwise know as a 1 oz. copper layer. The MCM contains a total of two thick metal layers and the rest are thin. One thick metal layer is on the component-side and the other is on the interconnect-side. Figure 6-5 provides an overview of the thin-film interconnect structure stack-up for these involved diamond MCMs.

Table 6-1. Diamond Substrate Materials Provided by Norton Diamond Film

Part Size (Diam)	No	Cust	Orig Due Date	Deposition Status	Proj Del Date	Disposition	Comments
3"	6	ESY Task 1	6/15/92	Complete.	TE174 (TI), TZ169 (TI), TE182 (ISR), TE161 (TI) shipped.	TE169 (SiN coated) remained at NDF for via fill. TE157 utilized for via-metallization prior to cracking. TE 201 at CRI for metallization.	TE201 will replace TA1074A.
4"	2	Cray Task 1	6/30/92	Complete.	TE193 & TE194 shipped.	TE194 diced for development.	
4"	2	Cray Task 1	10/31/92	Complete	TZ196 & TE196 diced and via-drilled.	Rejected but used for via-fill process development at CRI, NDF, & Thin Film Concepts.	
4"	2	Cray Task 1	12/31/92	Complete.	TE199 & TZ205 shipped.	TE199 and TZ205 shipped to CRI	
2" x 2" unloaded MCM	1	ESY	1/31/93		TBD	TA 1088A in reserve to be cut to 2" x 2" part.	Awaiting instructions from E-Systems.
4"	2	Cray Task 1	2/28/93	Complete	TA1067 &TA1082 shipped	TA1067 & TA1082 shipped to CRI	
4"	1	Cray Task 1	4/30/93	Complete	5/94	TA1207 rejected by CRI TA1237 shipped to CRI.	
4"	4	Cray Task 2	5/31/93	Complete.	TA1247, TA1237, TA1268, and TD1285 shipped	TA1247, NTA1-23 TA1268, and TD1285 shipped to CRI.	
4"	1	Cray Task 1	6/30/93	Complete.	TA1291 shipped	TA1291 shipped to CRI.	
4"	5	ESY Task 2	9/30/93	Complete.	TA1309 shipped	TA1172 cracked during lapping and replaced by TA1309, which has been shipped to TI.	4 of 5 to be replaced by AlN substitutes for Task 2.
4"	7	ESY Task 3	1/1/94	Complete	2/94, 3/94, 3/94, 4/94, 5/94, 5/94, 6/94, 6/94, 7/94, 7/94, 7/94, 7/94	NTA1-55, NTA1-58, NTA1-63, NTA1-74, NTA1-60, TA1484, and TA1529 shipped to TI.	
4"	2	Cray Task 3	1/1/94	Complete	4/94, 4/94, 5/94, 5/94	TA1362 and NTA1-38 shipped to CRI.	

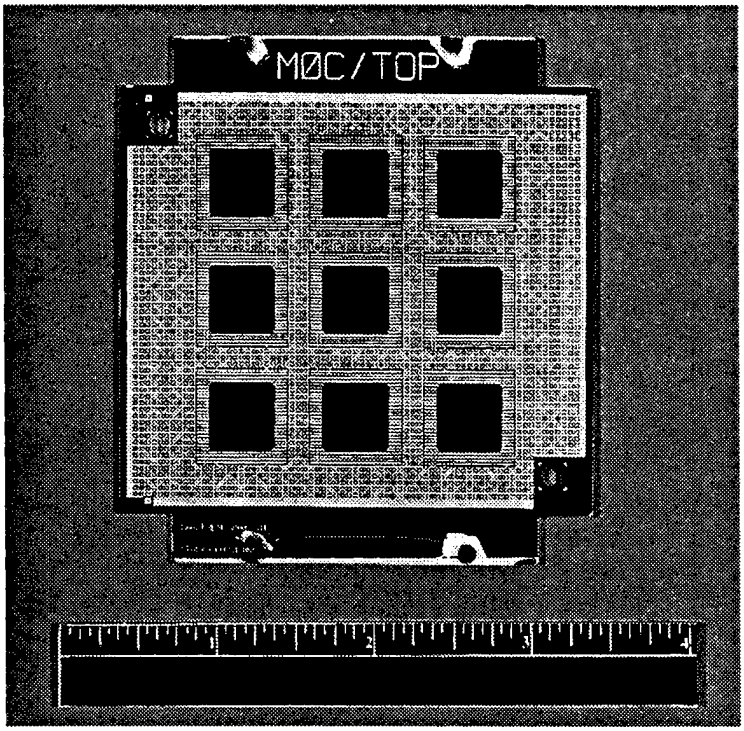


Figure 6-4. Metallized Diamond Substrate (Component Side)

Component Side

• M0	Plane (gnd)	18.3um Cr/Cu/Ni/Au
• M1A	Fanout Layer	4.5um Cu
• M1B	Routing	4.5um Cu
• M2	Thick Metal Plane	37um Cu
• M3	Pads Only	8.0um Ti/Cu/TiW/Au

Interconnect Side

• M0A	Plane (gnd)	18.3um Cr/Cu/Ni/Au
• M0B	Fanout	4.5um Cu
• M1	Plane (pwer)	4.5um Cu
• M2	Routing	4.5um Cu
• M3	Plane (gnd)	4.5um Cu
• M4	Routing	4.5um Cu
• M5	Thick Metal Plane (gnd)	37um Cu
• M6	Pads Only	8.0um Ti/Cu/TiW/Au

Total Nets: 1530 From-To's: 9159 Database Size: 102 Mbits

Figure 6-5. Thin-Film Interconnect Layer stack-Up

A nomenclature was developed to describe the MCM layers. The following paragraphs provide brief descriptions of the 13-metallization layers:

6.3.2.1 Component Side

M3 is a 'pads-only' thin metal layer that matches the fuzz button spacing and pitch associated with the fuzz button retainer boards. These pads are essentially "landing pads" for the fuzz buttons.

M2 is a thick metal layer that distributes the VEE1A, VEE1B, and VEE1C voltages. This layer is basically a pass-through layer for the vias from the pads-only layer. The thick metal is required for carrying up to 100 amps of current for the VEE1A and VEE1B voltages. VEE1C, which uses less than 3 amps, was also distributed on this layer.

M1B is a thin metal layer that provides X-Y routing capability on the component-side to facilitate signal fanout from the IC outer lead bond pads to the 20-mil grid vias in the diamond substrate.

M1A consists of an array of 15-mil square pads with each pad directly over a diamond substrate via. This thin metal layer provides a reliable interface between the M0 layer metallization and the component side HDI layers. This fanout layer contains pads that are positioned directly above the M0 layer with a via drilled at each corner. This provides maximum distance between the via drill sites and the diamond substrate via so as not to damage the interconnect structure during the via drilling process. No traces are routed on this layer.

M0 is a thin metal layer that is metallized directly to the diamond substrate and is used as a meshed ground plane. The diamond substrate vias are also plated through during this metallization process which provides the electrical connection through the diamond substrate. As shown in previous Figure 6-4, the M0 layer has a structure like a perforated plane to ensure that all trapped gases on the diamond surface would have an escape route, thus preventing bubbles from forming under the metal layer during processing. The CAD design formed the metal layer from a crosshatch of columns and rows of 5-mil wide traces and spaces. The pad sites were inserted in the crosshatched pattern at the positions of the diamond substrate vias.

6.3.2.2 Interconnect Side

M0A is a thin metal layer that is metallized directly to the diamond substrate and is used as a meshed ground plane. This layer performs the same function for the Interconnect side that the M0 layer does for the Component side.

M0B is a thin metal layer that performs the same function for the Interconnect side that the M1A FANOUT layer does for the Component-side.

M1 is a thin metal layer that distributes the VEE2A, VEE2B, and VEE2C voltages. It provides a reference plane for the adjacent M2 layer for controlled impedance routing.

M2 is a thin metal layer used as a signal routing layer for 50 Ω controlled impedance signal traces. This layer and layer M4 provide virtually all the signal routing for the MCM.

M3 is a thin metal layer that distributes ground across the MCM. This plane also is used as a reference plane for the two adjacent controlled impedance planes, M2 and M4.

M4 is a thin metal layer used as a signal routing layer for 50 Ω controlled impedance signal traces. This layer and layer M2 provide virtually all the signal routing for the MCM.

M5 is a thick metal layer that distributes ground across the MCM. It's a 1 ounce copper layer designed to carry up to 100 amps.

M6 is a "pads-only" thin metal layer. It's similar in function to the M3 on the Component side because it interfaces to the fuzz buttons of the adjacent Fuzz Button board. Unlike M3, M6 doesn't have die bond pads but it does have capacitor mounting sites. These capacitors provide de-coupling for the distributed voltages.

6.3.3 High Speed Test Chips

The integrated circuit chips used to furnish and control electrical signals within the MCM stack and for temperature sensing within each chip are high-speed test die designed and developed by Cray Research, Inc. Many of their operating parameters are proprietary to Cray. The chips are of two types, the Test Characterization (ti) die and the Clock (tz) die. The ti chip functions as a voltage-controlled current source and is capable of dissipating greater than 150 watts per chip. Figure 6-6 provides a summary of the key features of this special test die. It also has on-chip circuitry for pattern generation and data collection functions that support signal integrity evaluations over a nibble wide data bus that runs at a 500 MHz clock rate.

Raytheon's fabrication efforts centered on the attachment and wire bonding of these high-speed test chips to the involved diamond MCMs. Several adhesives were evaluated to determine which would be appropriate for attaching the chips to the diamond substrates. Areas of the HDI layers on the component-side of the MCMs are ablated away to allow the die to be directly attached to the diamond surface. Due to the high probability of rework and the differences in thermal expansion coefficients between diamond and silicon, a thermoplastic adhesive offered advantages over a thermoset adhesive. Consequently, a conductive, silver-filled film thermoplastic adhesive manufactured by Alphametals (Part # 571) was chosen. This adhesive has an extremely low Modulus of Elasticity (60,000 psi) allowing for reduced stress and greater compliance of the adhesive.

After die attach, the high-speed test chips were wire-bonded to the diamond MCMs using a Hughes 2460A automatic wire-bonder. Tests were conducted using 1-mil diameter gold wire. Satisfactory wire bond loops and ball diameters were achieved. Destructive bond pull tests were conducted which yielded bond pull strengths of 7.9 to 9.4 grams, significantly higher than the Mil Spec strength of 3.5 grams.

The ti and tz chips are approximately 400-mils square and 25-mils thick. Each chip has 384 I/O pads on a 4-mil pitch, and each pad is approximately 2-mil square. The die pads are wire-bonded to an array of pads that encircle each die. The outside HDI layer is a pads only layer and contains both the die bond patterns and the fuzz button land pads. The die bond patterns consist of two rows of 4 x 8 mil pads on 8-mil centers. These two rows provide sufficient density to support the 2 x 2 mil die bond pads on 4-mil centers. Figure 6-7 illustrates this pattern for the ti chip.

- CMOS/Bipolar-Type
- 1cm Per Edge Die Size
- ECL Compatible
- 500 MHz Clock
  - Signal Integrity Testing
- Programmable Power Variations
  - Thermal Integrity Testing
- Boundary Scan Network
- 384 Total Pins
- Integrated Temperature Sense Diodes
  - (10/die)
- Programmable Clock Delay

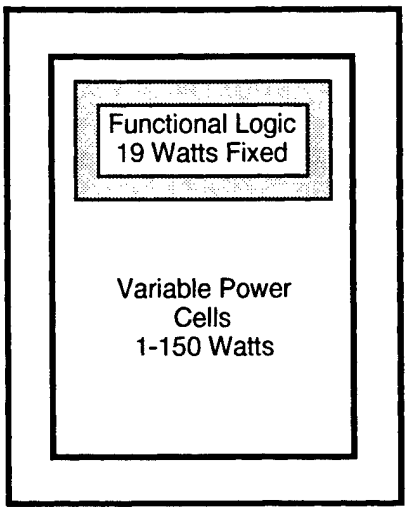


Figure 6-6. Special High Speed Test Die

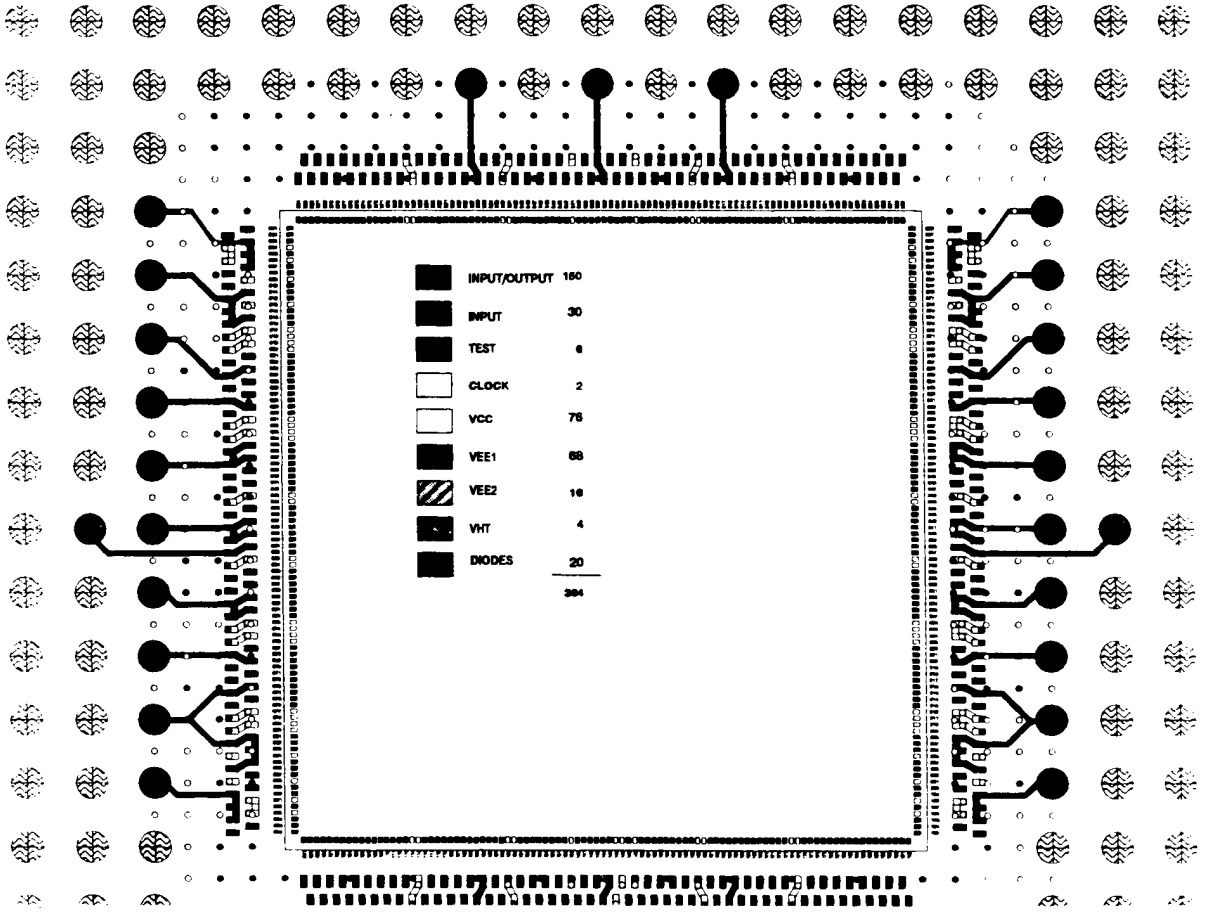


Figure 6-7. Test Chip "Fan Out"

6.4 Fabrication of Turn-Around Boards

The Turn-around Boards were designed to cap the top and bottom of the MCM stack in order to turn-around the signals coming from the stack and route them back into the stack. These boards require the 40-mil grid to interface to the fuzz button contacts associated with the Fuzz Button Retainer Boards in the stack.

Each turn-around board is an 8-layer printed circuit board, with two pads-only layers, two signal layers, two ground layers and two power layers. The four power planes (i.e. two power and two ground) are all 1 ounce copper planes. They provide extra copper for power distribution across the MCMs. This helps to minimize the voltage drop across the substrates. The signal layers are 50 Ω controlled impedance single-stripline layers used for the high-speed signal routing of the 500 MHz signals. BT epoxy is the laminate material used in the construction of the PCB.

To further assist in power distribution, the turn-around boards were designed to interface to an external bus bar that connects one side of the cube with the other side, thus, launching power in from both sides of the cube. This again works towards minimizing the voltage drop across the MCM by providing a low resistance path to the other side of the substrates.

7. SPRAY-COOLER ASSEMBLY

The spray cooling assembly used to extract the heat from the 3-D cube was designed and fabricated by Isothermal Systems Research, Inc. (ISR). Figure 7-1 provides a photograph of the completed cooling system integrated into the Demonstration Test Bed. The spray cooling system consists of a pump, condenser, coolant, sensors, two spray plates, and miscellaneous plumbing fixtures. A block diagram of this cooling system is shown in Figure 7-2.

The gear pump used to circulate the coolant is capable of delivering 80 grams/sec at 50 psi. The pump speed can be varied to adjust coolant flow rate.

The condenser is a custom designed water to fluorinert heat exchanger. It removes the heat from the heated fluorinert vapor and condenses it back to a liquid.

The coolant used is Fluorinert FC-87 manufactured by 3M. The coolant has a boiling point of 30 °C at atmospheric pressure. The Fluorinert fluids used on this program were thought to be inert. However, they have been proven to be non-inert. They can attack the plasticizers in the plastic materials used in the system by leeching out the silicon oils. When the liquid gets contaminated its heat extraction performance is dramatically reduced. The leeched oil is deposited on the surfaces to be cooled and prevents the vaporization the must occur to achieve the desired performance of the cooling system. Periodic replacement of the fluorinert used in the spray-cooler system was performed to minimize any performance effects due to contaminated cooling fluid.

The cooling system monitors temperature, pressure, and volumetric flow to aid in system set up, operation, and trouble shooting. Thermocouples are used to monitor temperature at the spray plate inlet, condenser inlet and outlet, and the water inlet and outlet. Output from the thermocouples can be fed to the data acquisition system for real-time monitoring during testing. A turbine type flow meter is located in the supply line to monitor volumetric flow rate. Fluid pressure is monitored at the supply header and the spray plate exit by analog gauges. A pressure transducer located at the fluid supply header feeds data to the data acquisition system. A low fluid indicator sounds an alarm if the fluid drops below a predetermined level. The location of these various temperature, pressure, and flow meters is shown in the block diagram of Figure 7-2.

7.1 SPRAY PLATES

The primary objective of the spray plate is to deliver atomized coolant droplets to the entire surface of the diamond fin that protrudes into the chamber. The spray plate developed by ISR contains 42 atomizers arranged in a 6 X 7 matrix. Each row of atomizers is angled 30° towards the diamond cooling fins and projects a 40° cone pattern as shown in Figure 7-3. This arrangement delivers a uniform elliptical coverage pattern when viewed normal to the fin edge. The number of atomizers, cone angle and angle of incidence were determined by ISR after several prototypes were built and tested. The final design provided full coverage of the diamond substrate fin. The 30° angle of incidence helped to flush coolant that did not vaporize out of the spray cavity. This kept the base of the fin, the area with the highest ΔT, available for direct impingement of the incoming coolant spray. An actual photograph of this spray pattern projecting from the fabricated spray cooling plate is shown in Figure 7-4.

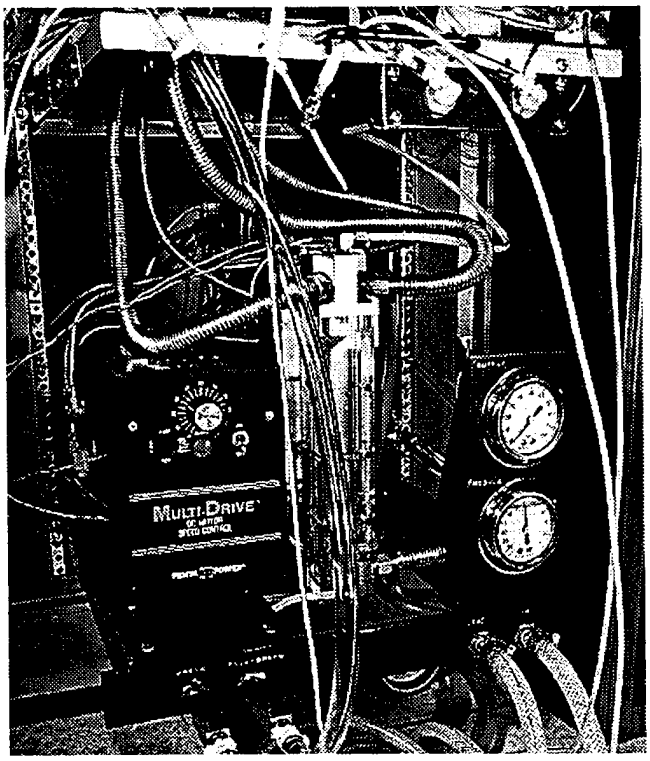


Figure 7-1. Spray-cooler System

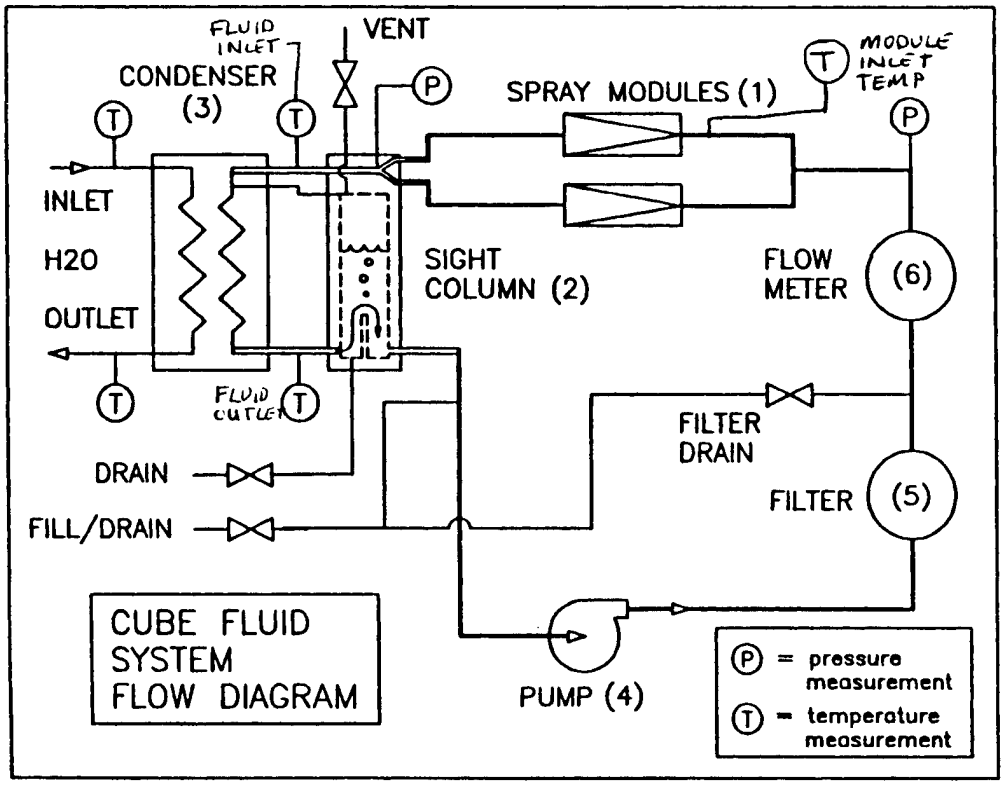


Figure 7-2. Block Diagram of Spray cooling System

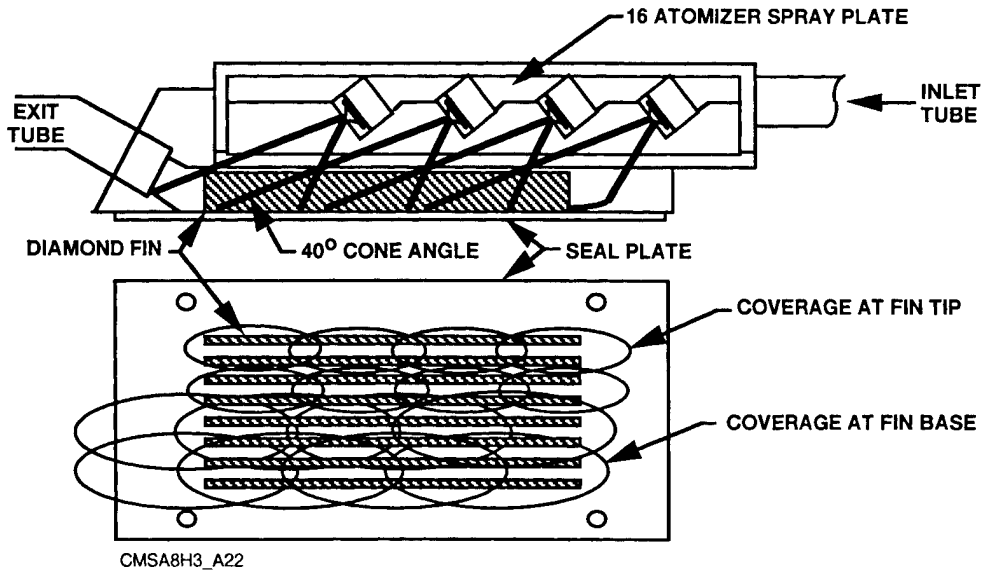


Figure 7-3. Spray Coverage Pattern of the Diamond Fins

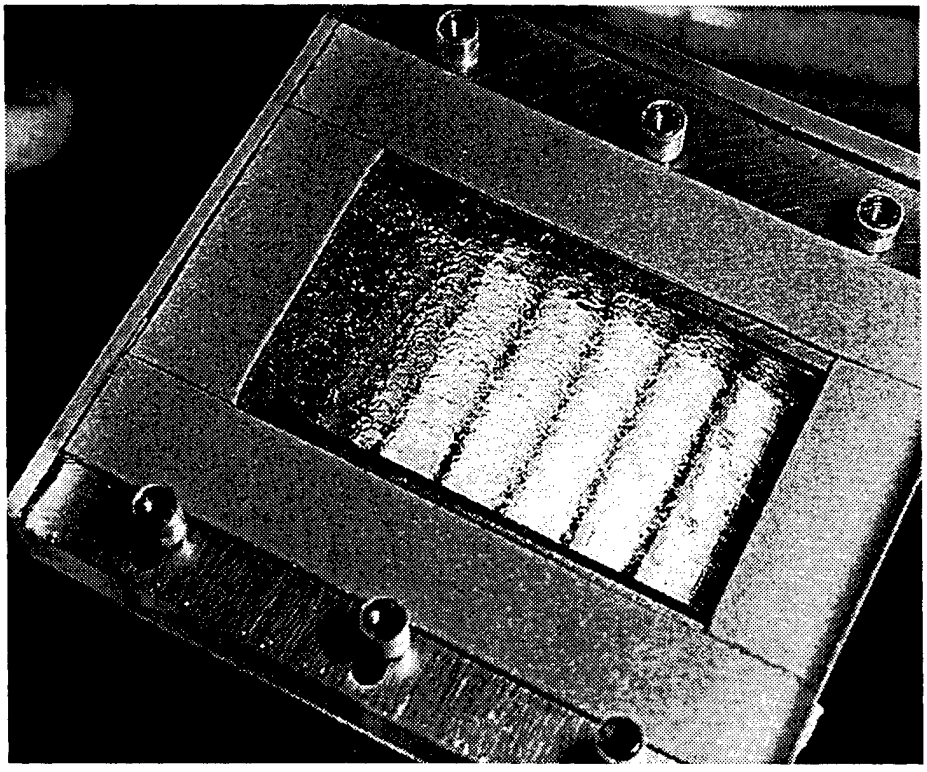


Figure 7-4. Fabricated Spray-cooler Plate with Spray Pattern

The heat transfer coefficient for this arrangement should be between 1.5 and 2.0 W/cm^2°C. This board edge spray cooling technique should be able to remove approximately 215 watts from each diamond fin, or 430 watts from each involved diamond MCM in the 3-D stack.

As shown in Figure 7-5, the holding fixture provides a surface to mount the spray cooling heads. The holding fixture has three studs protruding from the base of the fixture. These studs align the spray-cooler head during installation to prevent damage of the diamond substrate fins. The spray-cooler heads have three holes along the bottom flange to mate with the alignment studs on the holding fixture. The top platen of the holding fixture has three tapped holes that accept mounting screws. The top flange of the spray-cooler head has three vertical slots that mate with the three mounting holes in the top platen. These slots allow for tolerance build-up in the stack and expansion and contraction during temperature cycling.

The sealing of the cooler heads to the stack is accomplished by using a compliant acrylic tape. The tape is manufactured by 3M corporation as a structural joiner between metal, glass, plastic, and composite surfaces. The tape is rated for continuous use at 149°C. Fluid compatibility and sealing performance testing of the acrylic tape was done by ISR. After 350 hours of operation at room temperature in fluorinert liquid, there was no sign of swelling, separation, or discoloration. The test specimen was then pressurized to 10 psi and no leakage was observed.

During the assembly of the stack a piece of 10-mil thick tape by 80-mil wide is placed along the entire edge of the substrate at the base of the fin. The tape thickness is the same as the fuzz button protrusion from the fuzz button retainer board. Prior to compression of the stack the tape contacts the MCM and the adjacent rigid/flex retainer board. As the fuzz buttons are compressed the tape is also compressed forming the seal. The tape is applied around the perimeter defined by the fins. The spray head is then attached to the holding fixture and the mounting screws are tightened. As the screws are tightened the tape is compressed creating the seal. Figure 7-6 provides a composite sketch of this process for sealing the spray heads to the 3-D cube assembly.

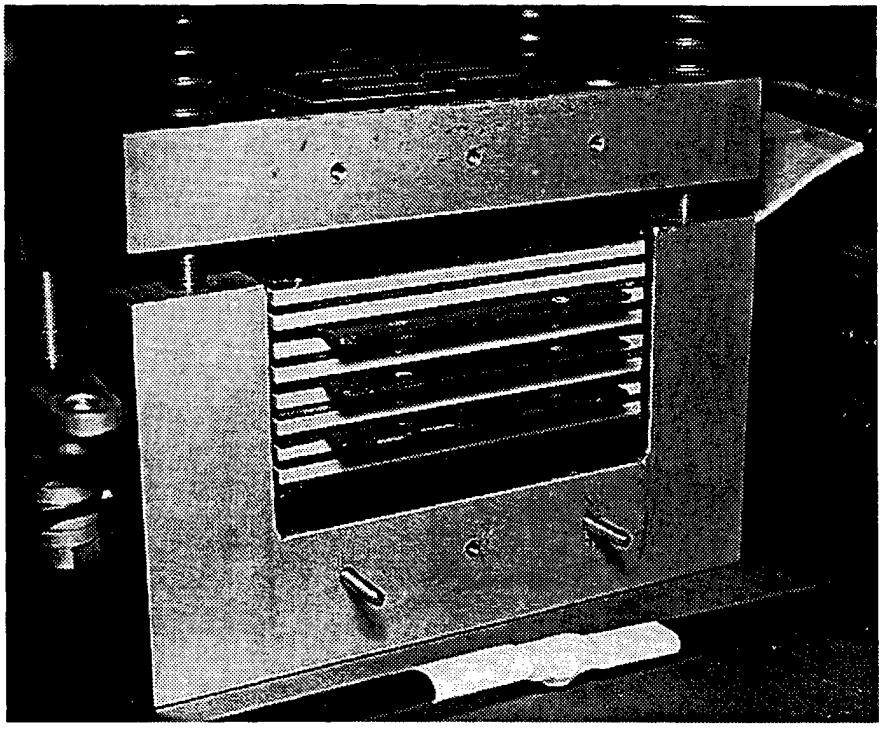


Figure 7-5. Diamond MCM Cooling Fins protruding from 3-D Stack

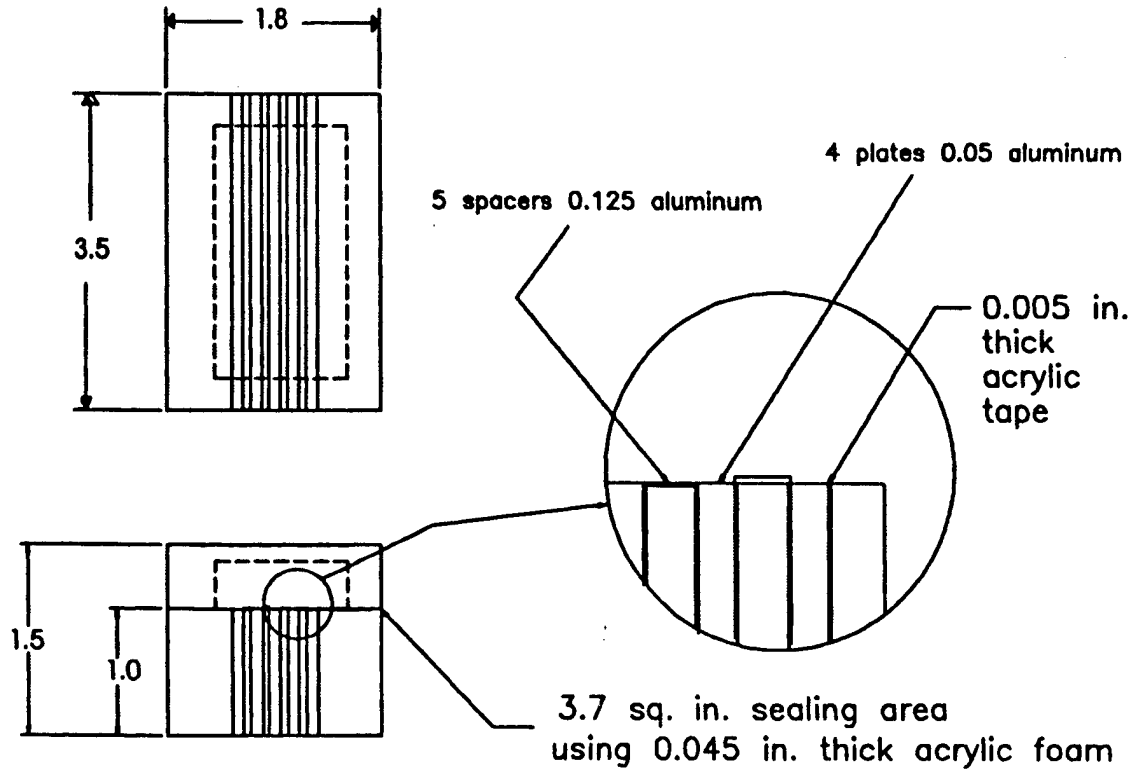


Figure 7-6. Spray Plate Fluid Sealing Process

8. TEST AND INSTRUMENTATION SYSTEM

The primary objective of the Demonstration Test Bed is to demonstrate the viability of diamond MCMs combined with the board-edge spray-cooler technology to perform thermal management under high power conditions. A second objective is to demonstrate the viability of packaging the MCMs in a 3-D configuration to enhance the high frequency performance of the cube assembly. Verification of the integrity of the 3-D Diamond MCM Cube assembly begins with the development of a global test strategy, and then designing and building a test and instrumentation system that will readily implement and report or summarize the results of that strategy. The global strategy for this verification is summarized in Figure 8-1. After fabrication and assembly of the cube assembly, simple mechanical integrity checks are first performed to determine the robustness of the z-axis interconnect structure. Following this, isolated electrical and thermal integrity tests are then performed. Finally, total system tests are performed combining thermal and electrical tests simultaneously.

To meet these objectives, Figure 8-2 provides a visual design overview of the test and instrumentation system that was integrated around the cube assembly. The key assemblies of this instrumentation system include:

- Test I/O Board
- Multiplexer/Signal Conditioner
- Power Supplies
- Host Computer

The following sections highlight the key design and implementation features of these test and instrumentation assemblies.

8.1 TEST I/O BOARD

The Test I/O Board is a double-sided surface mount, 12 x 14-inch multi-layer printed circuit board. It provides the circuitry necessary to interface the host computer and the thermal and signal integrity test hardware to the MCMs in the 3-D stack. The block diagram in Figure 8-3 illustrates the basic functions performed by this board and includes:

- GPIB Interface
- Main Controller
- Nibble Data Bus Interfaces
- FIFO Pattern Buffer
- Signal Fan Out
- System Clock Distribution

8.1.1. GPIB Interface

The Host Computer communicates to the Test I/O Board via a GPIB Interface (i.e. IEEE 488 bus). This interface circuitry was copied from an existing design with only slight modifications. An Altera Field Programmable Field Array (FPGA), along with some standard interface ICs, provide the necessary handshake control.

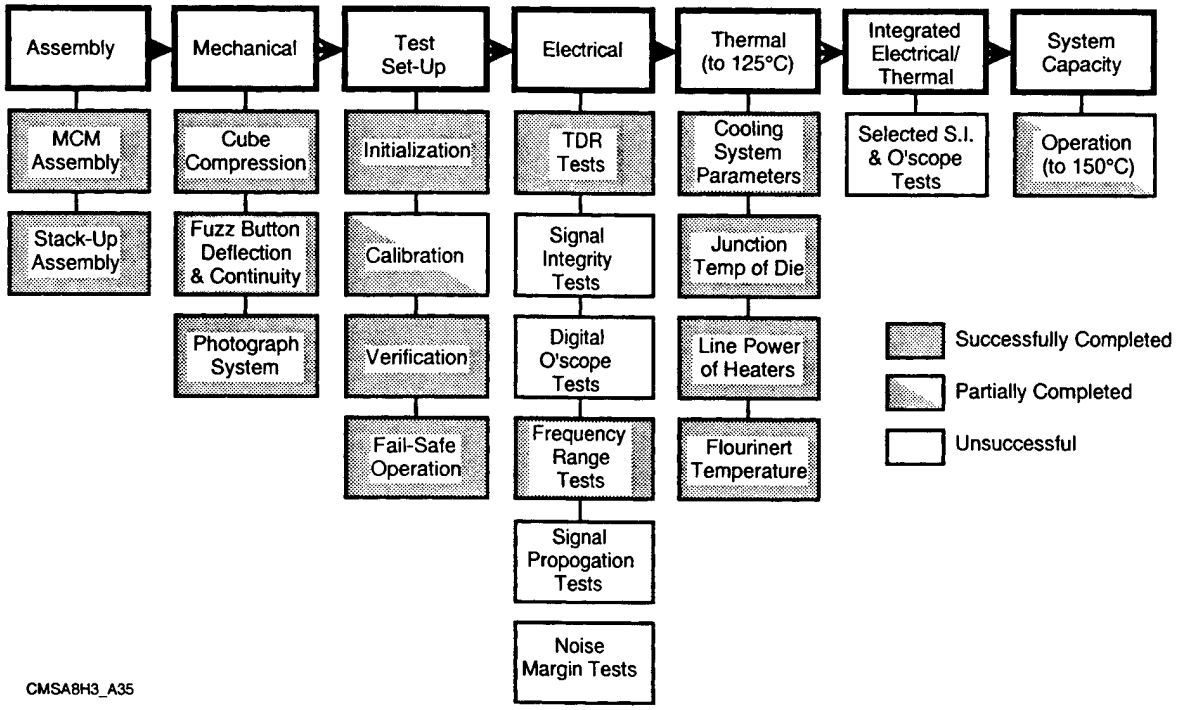


Figure 8-1. Test Plan for the Demonstration Test Bed

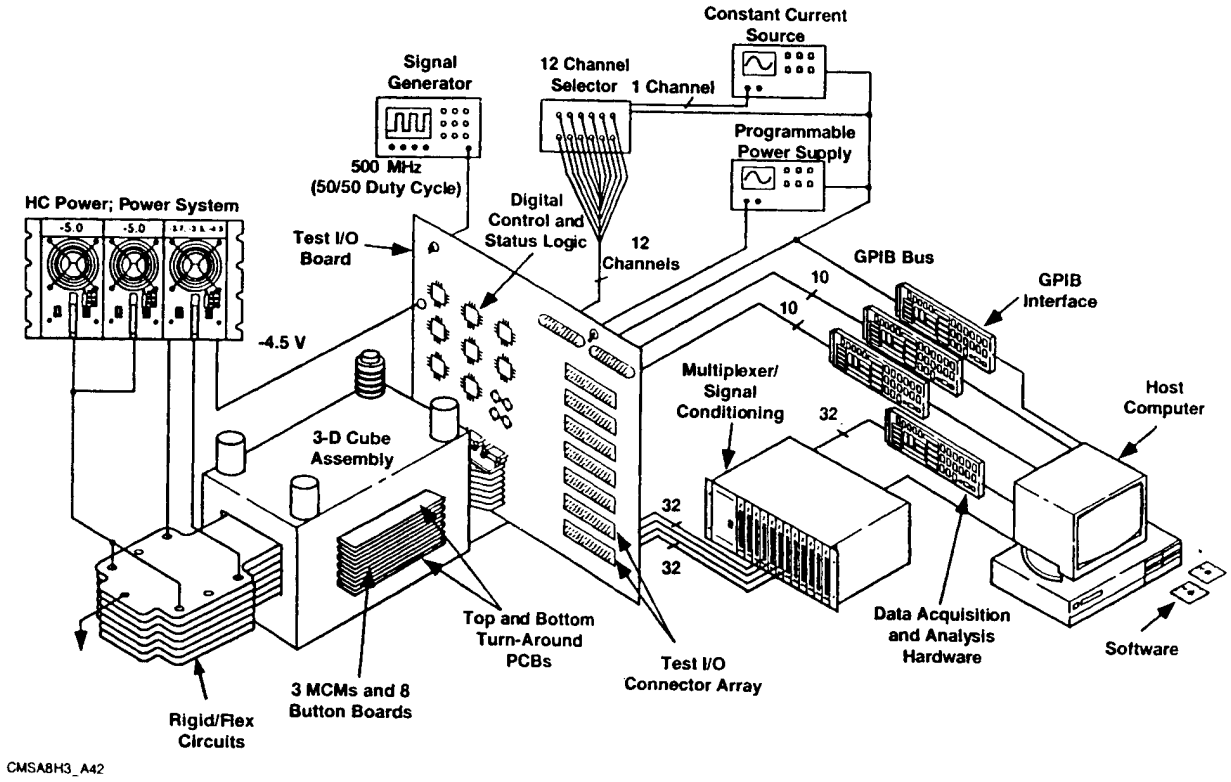


Figure 8-2. Functional Overview of Test and Instrumentation System

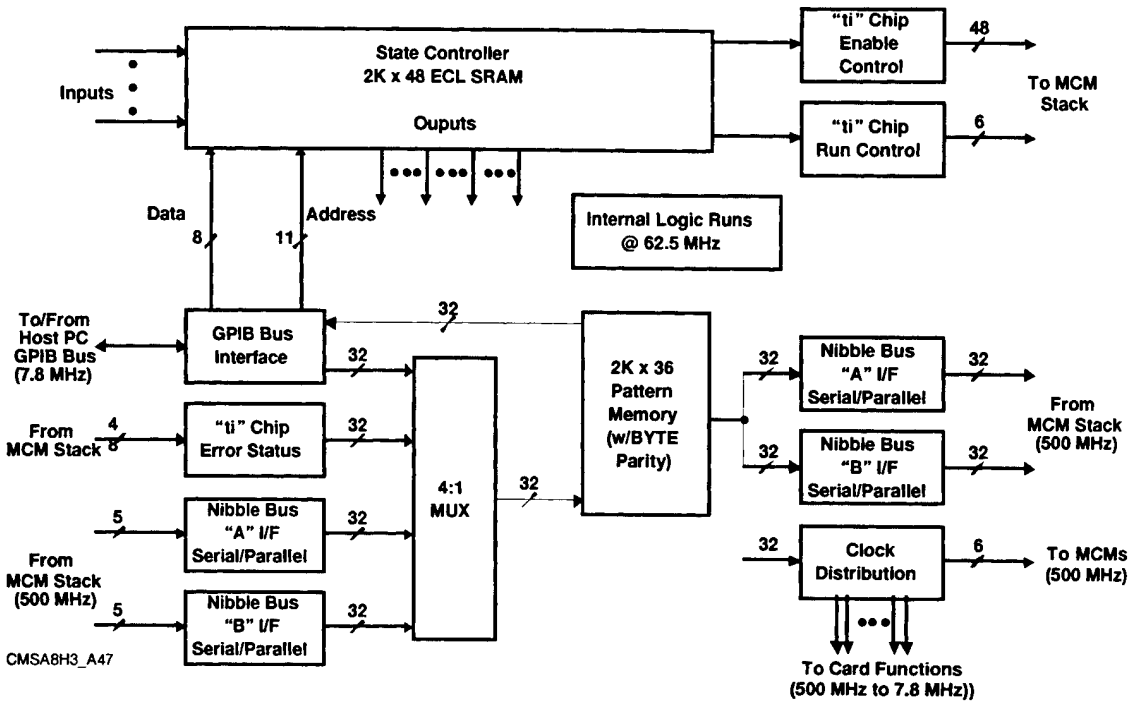


Figure 8-3. Test I/O Board Block Diagram

8.1.2 Main Controller

The Main Controller function for the Test I/O Board is implemented in the Altera Field Programmable Gate Array (FPGA). This controller reads the status signals from the MCMs, controls the GPIB interface, controls the pattern data FIFO Pattern Buffer, and provides control lines as necessary to facilitate communications to the MCMs in the 3-D Cube Assembly. When data is downloaded from the host computer, every data byte is preceded by a control byte. The control byte provides the Main Controller all the information needed to process the data byte contained in the next byte received over the GPIB. The control byte also commands the Main Controller to perform execution functions such as "START TEST", "COLLECT STATUS", "RESET", "TRANSFER DATA TO CUBE", "UPLOAD DATA FROM CUBE", etc.

In a normal operation, the Main Controller begins receiving control and data bytes across the GPIB. To setup a test, each data byte following the control bytes is transferred and stored in the FIFO Pattern Buffer. When this download is complete, the Main Controller receives a "START TEST" command from the Host Computer. The controller then commands the FIFO Pattern Buffer to send the data pattern to the "ti" chips on the MCMs and begin the test operation.

8.1.3 Nibble Data Bus Interfaces

The Nibble bus consists of four bits of parallel data plus a data valid signal that surrounds the valid data. All five signals are differential, resulting in 10 wires per nibble interface. The 3-D Cube Assembly contains two independent nibble bus loops. Each loop requires an output bus and an input bus. Each nibble bus is a daisy-chained communication loop that links the "ti"

chips and Test I/O Board together. The output nibble bus is driven by the Test I/O Board and connected to the input nibble of first "ti" chip in the loop. Then, the first chip connects its output nibble bus to the input bus of the next "ti" chip in the loop. This continues until the last chip is connected to the loop. Then the output bus of the last chip in the loop is connected to the input bus of the Test I/O Board, which completes the loop. If more than one MCM is present in the 3-D stack, then the loop continues through each MCM until the last MCM in the stack outputs to the Test I/O Board. In the case of two or more MCMs, the last "ti" chip on the first MCM outputs to the first "ti" chip on the next MCM. This continues the daisy chain through the entire 3-D stack. If connection failures occur in the loop, then half of the "ti" chips in the stack are inaccessible to the Test I/O Board circuitry. However, tests can still be run on the second daisy-chain loop of "ti" chips in the cube.

8.1.4 FIFO Pattern Buffer

The Test I/O Board interfaces the FIFO Pattern Buffer to the output nibble busses via a 32-bit parallel to 4-bit parallel conversion. The 32-bit data word is read out of the FIFO memory at 62.5 MHz and parallel-to-serial converters multiplex the data onto a 500 MHz 4-bit parallel nibble bus. This nibble bus is then distributed to provide two separate outputs that interface to the two independent nibble loops of the 3-D stack.

The Test I/O Board interfaces the FIFO Pattern Buffer to the input nibble busses via a 4-bit parallel to 32-bit parallel conversion. The 4-bit data word is received from the stack on a 500 MHz nibble bus and converted to a 32-bit word at 62.5 MHz and written into the FIFO memory. An input multiplexer to the FIFO memory determines which nibble bus will provide data to the memory for storage.

The FIFO Pattern Buffer consists of four 2K x 9-bit FIFOs arranged into a 2K x 36-bit memory bank. The 36-bit word consists of 32 bits of data with four bits of control. The chips are clocked by a 62.5 MHz clock (i.e. 500 MHz divided by eight). The FIFO Memory operations are controlled by the Main Controller.

8.1.5 Signal Fan Out

The Test I/O Board provides a signal fan out of the analog signals that monitor and control the heater functions of the "ti" chips. The signal fan out connects these signals from the high-density connectors of the Rigid/Flex Circuit to the lower density connections of the 96-pin DIN connector array on the Test I/O Board. Each MCM provides connections to 80 thermal diodes on the "ti" and "tz" chips. Each MCM also provides connections to 32 VHT signals that provide the voltage control for the current sources of the "ti" chips. In a full 3 MCM 3-D stack, a total of 243 diode signals and 96 VHT signals require connection to either sense lines or control signals. These signals interface to the data acquisition and peripheral hardware used to monitor and control the heater functions.

8.1.6 System Clock Distribution

The Test I/O Board provides the System Clock Distribution for the Cube Assembly and Demonstration Test Bed. It receives a 500 MHz signal from a signal generator, distributes it to the MCMs and parts of the Test I/O Board, and divides the 500 MHz signal down for

distribution to the slower speed sections. Each MCM clock or "tz" chip receives an ECL–level differential clock from the clock distribution function on the Test I/O board. The distributor outputs can be ganged together to provide a total synchronous system or they can be provided separate clocks to simulate an asynchronous system. Z-axis signal routing through the stack accomplishes the task of routing synchronous signals with asynchronous ones for crosstalk and noise margin assessments.

8.2 MULTIPLEXER/SIGNAL CONDITIONER

The Multiplexer/Signal Conditioner acts as a large analog multiplexer for conditioning of test signals received from the Demonstration Test Bed and routing them to the Host Computer for analysis and display. The conditioned signals include the temperature sensor diode readings from each MCM in the 3-D stack, various temperature readings from thermocouples surrounding the Cube Assembly, and fluid flow and supply sensors associated with the Spray-cooler Assembly.

This function is implemented by means of the SCXI-1100 module that is part of the Instrumentation Series modules from National Instruments® data acquisition plug-in boards. The SCXI-1100 has been populated with four data acquisition (DAQ) and conditioning modules to provide a total 128-channel differential input multiplexer with programmable gain control, buffering and data protection. Figure 8-4 shows the allocation of the various diode and sensor data channels to the four involved DAQ modules comprising the SCXI-1100.

This multiplexer has a digital section for automatic control of channel scanning and calibration. For the Demonstration Test Bed, all 128-channels are scanned every six seconds and passed on

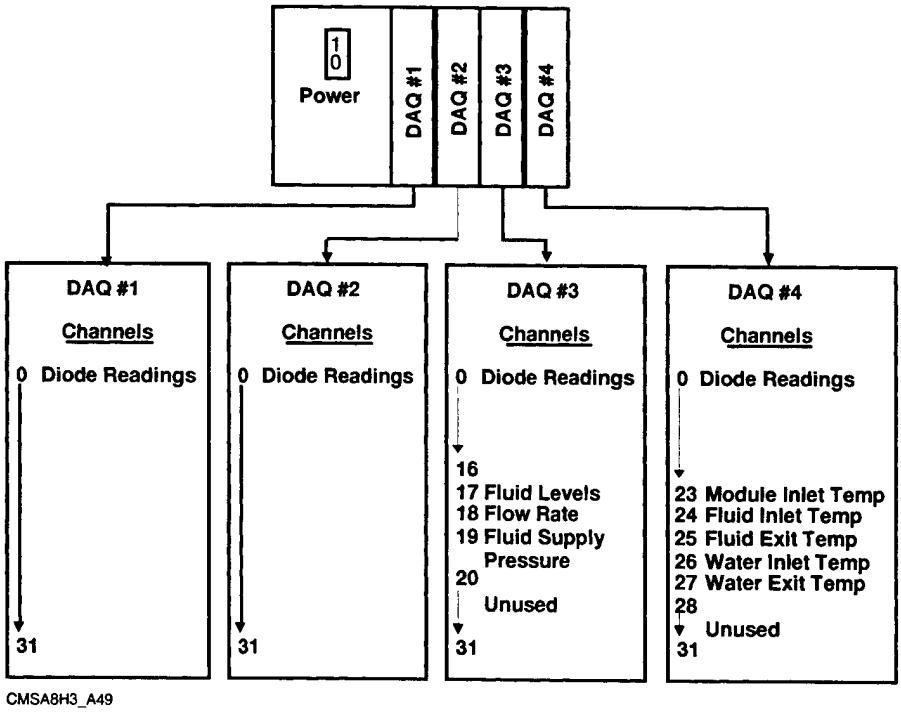


Figure 8-4. Configuration of Data Acquisition Channels

to the Host Computer. In the Host Computer, a comparable I/O board has been inserted for timing control and communication with the SCXI-1100. This I/O board is National Instruments AT-MIO-16F-5 that has full PC I/O channel DMA capability with 256-word A/D FIFO buffer. Communication between the multiplexer and the I/O board in the Host Computer is by means of National Instruments SCXIbus. The SCXI-1100 connects to the SCXIbus via a 4x24 metal receptacle on the chassis rear, and all data acquisition inputs are provided to the chassis front by means of a 50-pin ribbon cable.

8.3 POWER SUPPLIES

Power is supplied to the MCMs in the cube assembly by a custom power supply manufactured by HC Power Inc. The power supply is a 220V 3-phase rack mountable unit. The power supply is capable of providing approximately 5kW of power to the cube. The output voltages and their corresponding maximum currents are as follows:

- two 5.0V @ 300A
- two 2.7V @ 300A
- one 5.0V @ 40A
- one 5.2V @ 40A
- one 3.5V @ 10A
- one 2.7V @ 5A
- one 2.0V @ 10A.

The 2.7V and 5.0V 300A outputs are used to supply power to the heaters (VEE1A, VEE1B) for the low and high power settings. The 5V, 5.2V, and 2.0V outputs supply power for the test I/O board, while the 3.5V, 2.7V, and 5.0V outputs supply power for the logic on the test die.

High current power is routed to the cube assembly via heavy gauge welding cable. The cables are attached to the power distribution area of the rigid/flex circuit with a vertical power buss. The copper in the rigid/flex circuit is designed to carry 100A for each of the power circuits (200A total per flex circuit). Figure 6-1 in previous Section 6.0 displays these power cables attached to the left side of the rigid/flex circuits embedded in the 3-D stack.

The rigid/flex circuit is connected to the MCM via a fuzz-button array. Since the power is supplied to only one side of the flex-circuit, an additional buss bar is provided around the outside of the clamping fixture to ensure uniform voltage distribution across the MCM.

The power supply and distribution as designed is capable of supplying over 3kW to a 6 MCM stack, even though only three MCMs were utilized in the fabricated cube assembly.

8.4 HOST COMPUTER

The host computer for the Test and Instrumentation System consists of an IBM PC (386/25 MHz with a math coprocessor). This computer is responsible for total system command and

control including the activation and sense reading of the temperature sensing diodes associated with each MCM in the Cube Assembly. In addition it commands adjustments of the controllable heater and signal sources with the Test Characterization die populated with each MCM.

Control interface is provided through GPIB Bus cards to the Test I/O Board and the various programmable power supplies and instrumentation equipment associated with the Test Bed as identified in previous Figure 8-3.

8.4.1 Man-Machine Interface

The human command and control interface with the instrumentation system is through a series of control menus implemented by means of a LABVIEW® software application package on the host computer. Five kernel menus perform this function and are identified as follows:

1. Main Menu
2. Mechanical Sensors
3. Diode Calibration
4. Diode Scan
5. Signal Integrity Tests

Interaction with these menus is by mouse pointer or through the computer keyboard. Specific commands for the instrumentation system that can be implemented include:

- Turn-on/system initialization
- Branch to other control menus
- Execute calibration procedures for temperature sensing diodes
- Set-up and control "Heater" voltages to "ti" chips
- Execute diode temperature monitoring (low power case)
- Execute diode temperature monitoring (high power case)
- Display/monitor diode temperatures
- Display/monitor thermocouple sensors (with alerts and flags)
- Display/monitor spray-cooler fluid flow rate, pressure, and fluid level sensors (with alerts and flags)
- Display/monitor signal integrity test patterns
- Update tables and variables associated with signal integrity test patterns
- Generate and store test results to disk
- Perform power-down/system off

All of these command and control functions can be implemented with these five basic kernel menus identified earlier. Figures 8-5 through 8-9 provide copies (screen dumps) of these operational menus.

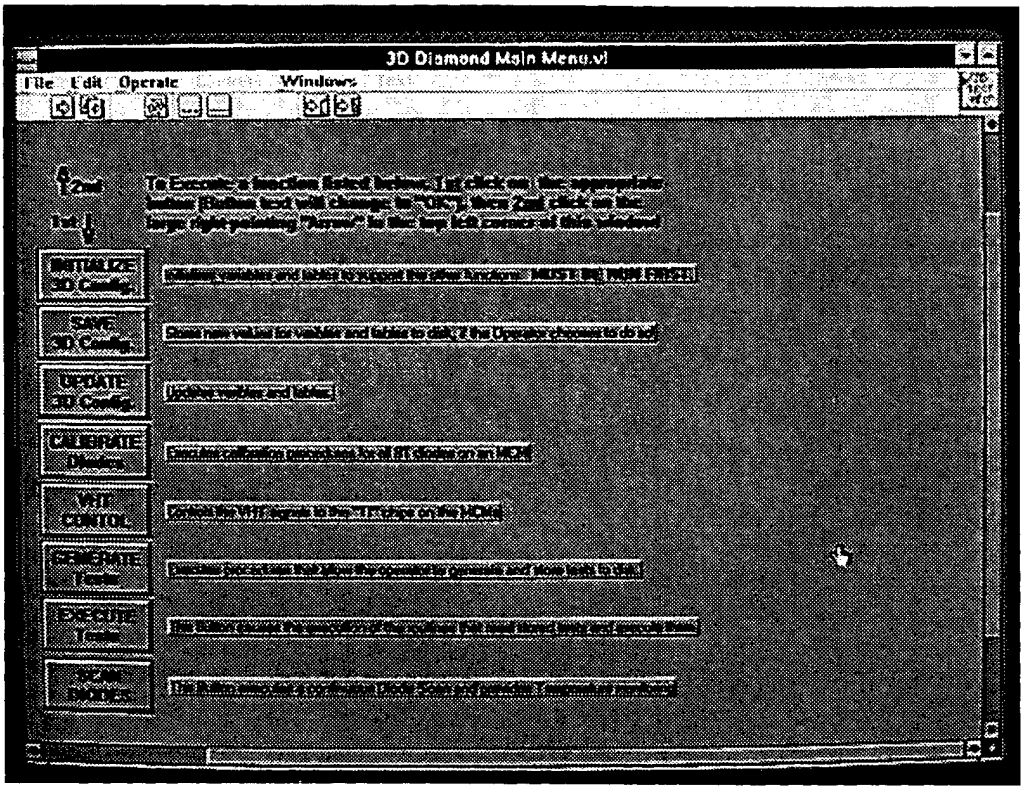


Figure 8-5. Main Menu

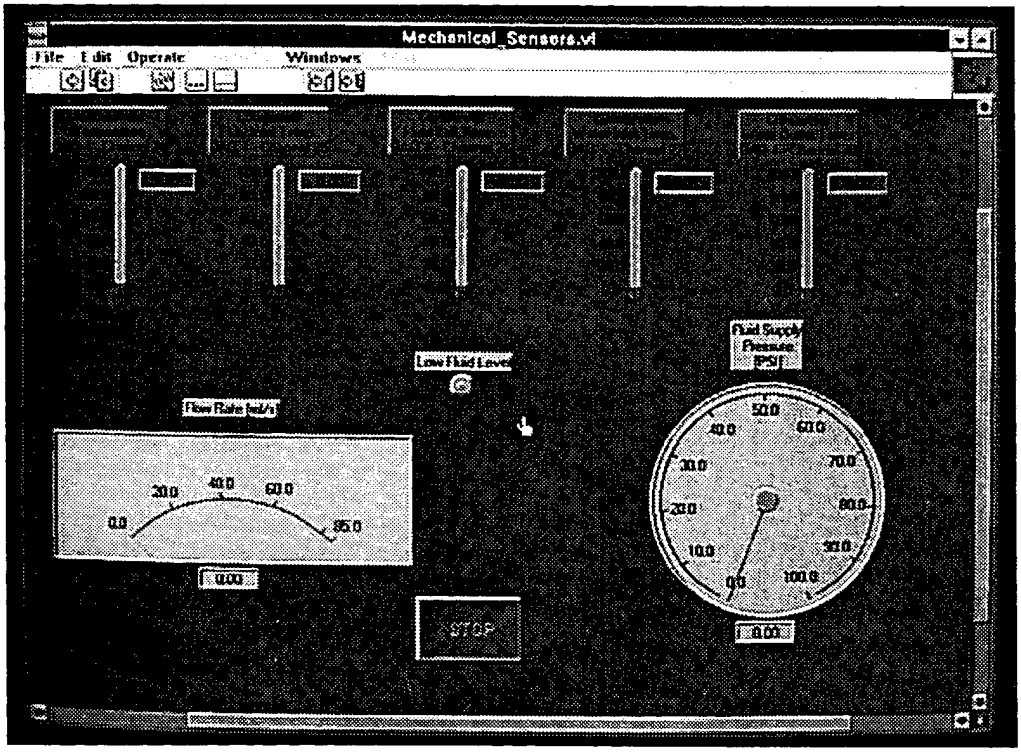


Figure 8-6. Mechanical Sensor Menu

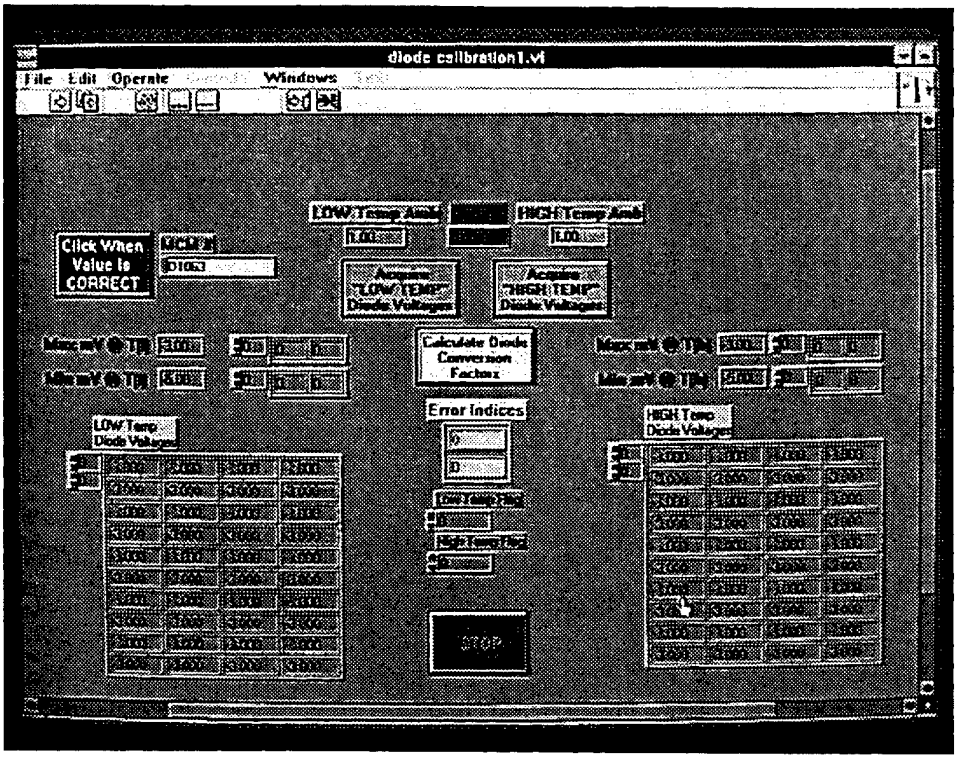


Figure 8-7. Diode Calibration Menu

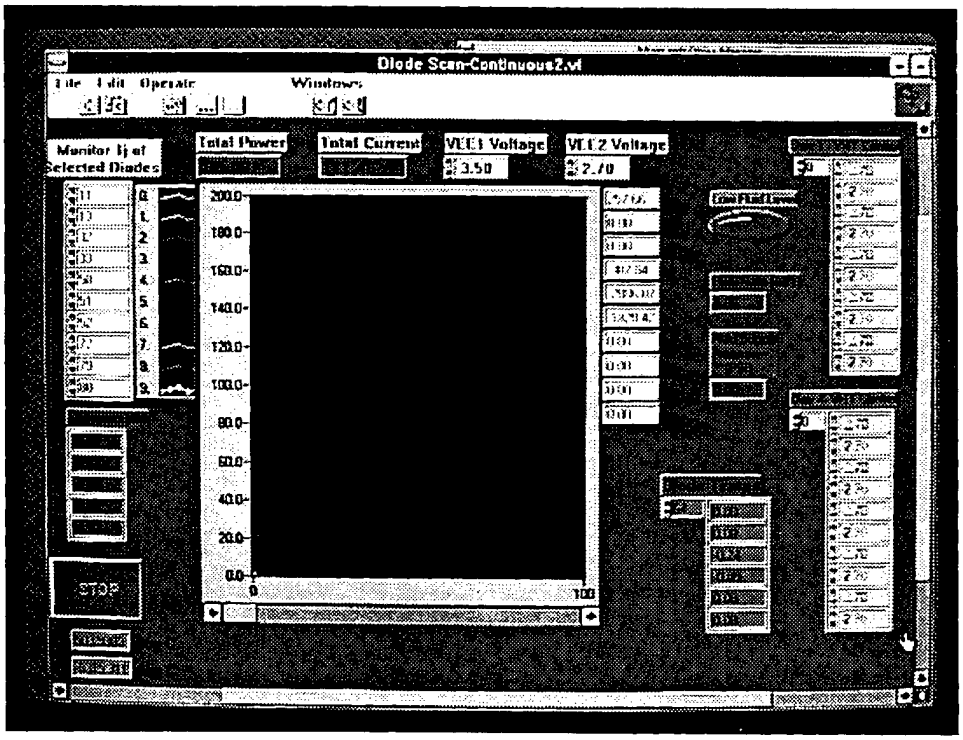


Figure 8-8. Diode Scan Menu

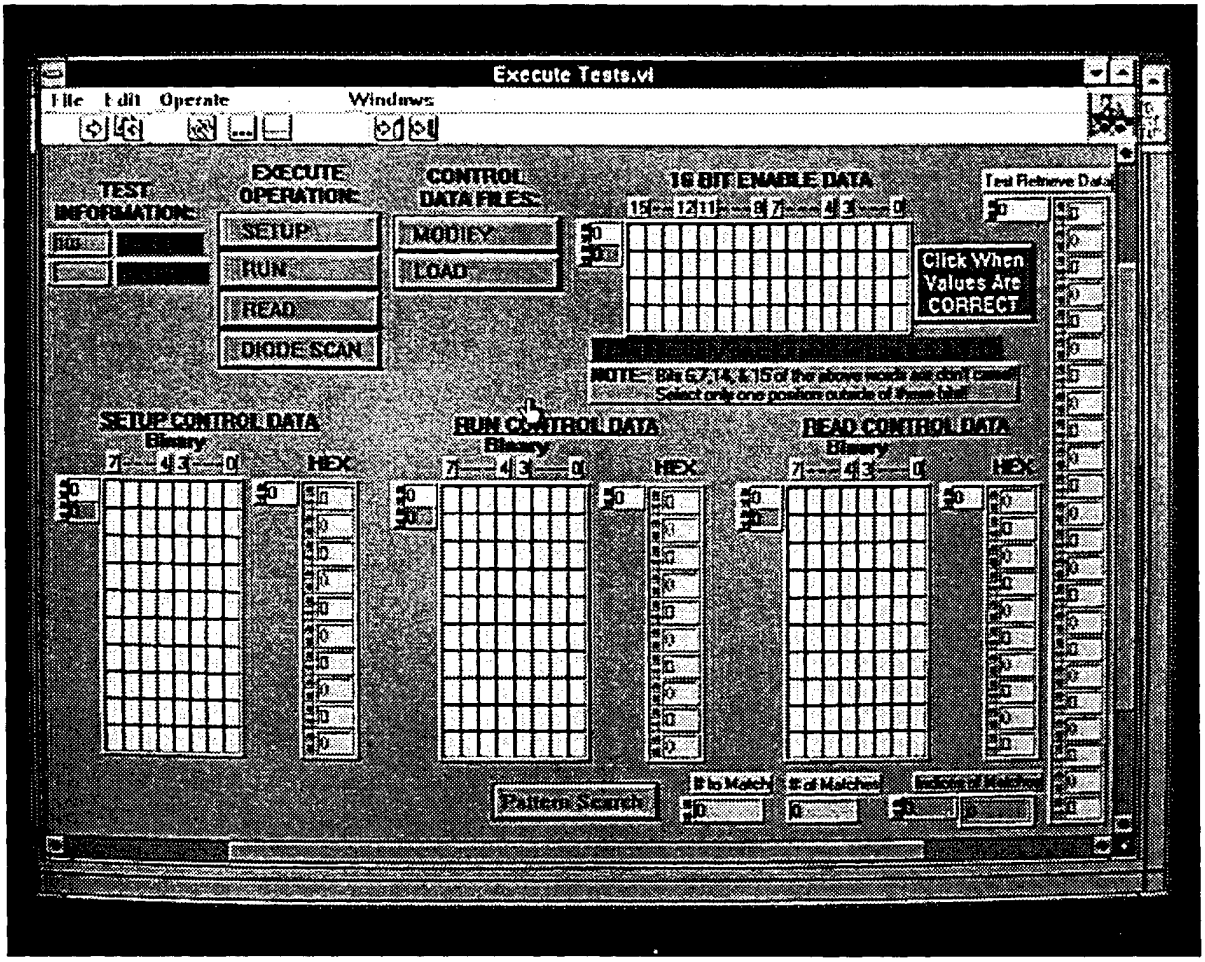


Figure 8-9. Signal Integrity Tests

9. SIGNAL INTEGRITY ANALYSIS

The integrity of digital signals propagating on the vertical (z-axis) interconnects and structures described in the previous sections may be quantitatively evaluated. The task every designer faces in high speed interconnects is in guaranteeing that signals are propagated between ICs throughout the 3-D MCM assembly with acceptable (minimum) levels of distortion. Ultra high performance for the 40 board system means ECL signal levels operating up to 1GHz clock speeds, having 60 ps rise and fall times.

Given the signal demands outlined above, the vertical interconnect structure must be thought of in terms of a "propagation medium," utilizing the concept of characteristic complex impedance, signal bandwidth, and time delay as frequently employed in microwave design. These vertical interconnects must be treated as a transmission line, characterized by its impedance, loss, and electrical length. The impedance of the signal sources and signal loads must also be considered. In general this network can be modeled by distributed resistance, inductance, and capacitive elements.

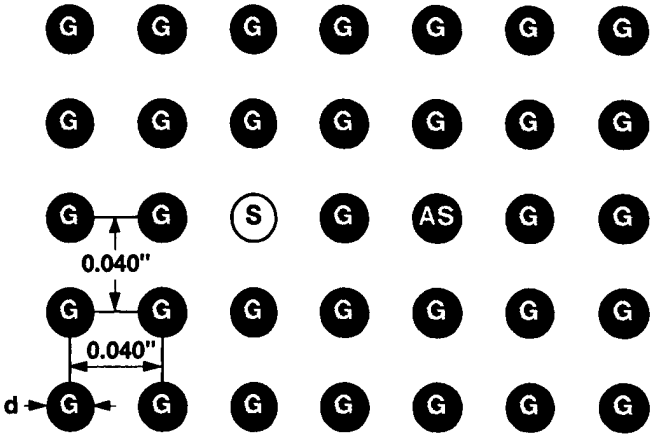
9.1 TRANSIENT ANALYSIS

A time domain transient analysis was performed to determine characteristic impedance, signal bandwidth, and time delay for one complete top to bottom interconnect path through all 40 MCM diamond substrates and spacer boards stacked vertically in the cube computer concept. This simulation analysis was performed using the XFX® and XNS® analysis software from Quad Design Technology, Inc.[2]. A true 3-D field solver would be more ideal for this analysis. The Quad Design tools were chosen since they were available and could be adapted to meet the objectives of this transient analysis by proper application of the 3-D circuit model representing each of the 40 cells comprising the vertical interconnects.

The transmission line parameters of each physical cell or vertical line segment were first determined using the 2-D field solver XFX®. The physical model for one vertical cell is shown in Figure 9-1. Each cell contains three elements:

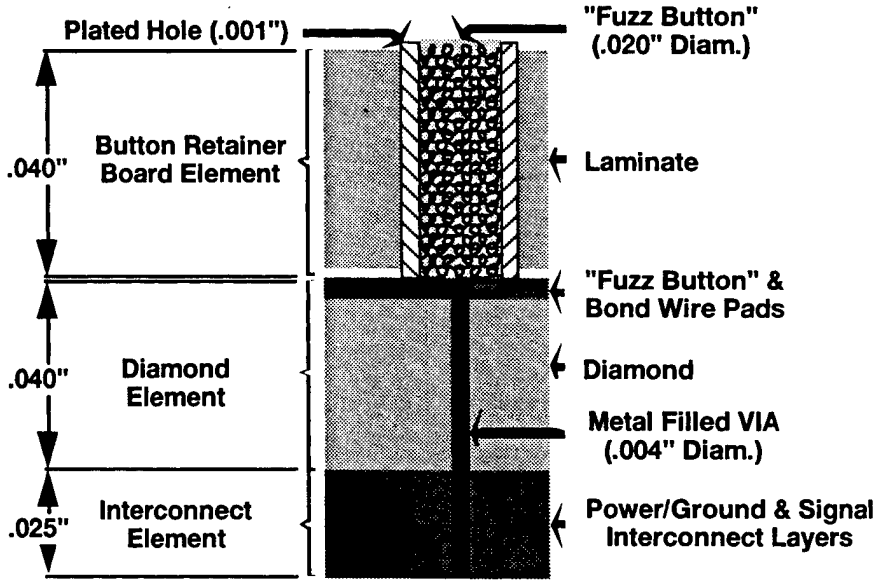
- A fuzz button spacer board
- A diamond substrate
- An x and y interconnect layer

[1] Quad XFS (Transmission Line Parameter Analysis) and XNS/TLC (Transient Analysis) software programs are copyright CAD tools of Quad Design Technology, Inc.



G = Ground
S = Signal
AS = Alternate Signal
d = Cell Diameter

Array of Vertical Cells (Top View)



DS9209-6©

Physical Cell (Side View)

Figure 9-1. Vertical Interconnect Model used in Field Solver

A 5 x 7 diagonal square array of these cells was also input to the field model to represent a signal isolation pattern for these vertical interconnect structures. Notice in Figure 9-1 that a signal was assigned to one of the center cells and the remaining 34 were grounded. The alternate signal (AS) conductor can be utilized by the field model to assess crosstalk. The fuzz buttons and metal filled vias had diameters of 20 mils and 4 mils, respectively. Three separate runs were performed

with the field solver, one for each element, to transmission line parameters per unit length Table 9-1 presents these resulting parameter values. These generate the parameters include inductance (L) and capacitance (C) per inch, dc resistance (Rdc) and skin effect (R_{skin}) resistances, and its characteristic impedance (Z_O).

Table 9-1. Transmission Line Parameters for One Cell

3-D MCM Element	Dielectric Constant	L (nh/in)	C (pf/in)	Z_O (Ω)	R_{skin} (Ω-ns^.5)	Rdc (Ω)
Fuzz Button Board	3.1	6.069	3.667	40.68	0 083	0.002
Diamond Layer	5.6	16.322	2.463	81.41	0.302	0.073
Interconnect Layer	3.5	16.322	1.539	102.98	0.302	0.073

The circuit diagram shown in Figure 9-2 was input into XNS® to perform the transient analysis of a signal vertically transmitted through 40 MCM cells stacked on top of each other. The ideal voltage source (V_S) drives ECL levels with 60 ps rise and fall times and a pulse duration of 2 ns. The source resistance (R_S) and capacitance (C_S) values simulate the output characteristics of a true ECL driver. Each box represents an MCM element in the signal path and states the appropriate lengths of each segment. The lumped capacitances, C_{f1}, C_{f2}, and C_{f3}, represent the fringe capacitance at the line segment interfaces as shown in Figure 9-3. These fringe capacitances were calculated with a 2-D field solver in cylindrical coordinates using a custom software package[3]. The load resistance (R_L) provides a matched impedance load. This circuit assumes an ideal ground return path and does account for skin effect and dc resistances. The calculated fringe capacitance caused by the non-uniform geometry at each element interface (conductors passing through ground planes) is tabulated in Table 9-2.

Table 9-2. Element Interface Fringe Capacitance (One Cell)

Element Interface	Term Definition	C (pf)
Fuzz Button - to - Diamond	C_{f1}	0.028
Diamond - to - Interconnect	C_{f2}	0.008
Interconnect - to - Fuzz Button	C_{f3}	0.025

These fringe capacitances and other transmission line parameters for the equivalent 40-cell circuit were input to XNS® to simulate a transient response. Figure 9-4 illustrates the waveforms of

[3] Private communication between Don Marshall and Richard Eden with extensive improvements made by Eve Shen

the 2ns pulse at both the source and load positions. Notice that the 60ps rise time is preserved indicating adequate signal bandwidth for this vertical interconnecting structure. The propagation delay (t_p) through the 40 cells is approximately 840ps. The characteristic line impedance (Z_o) was calculated by averaging the impedance's of the three elements of each cell together. Thus, the total capacitance (C_T) and inductance (L_T) of a cell was determined and Z_o was calculated using

$$Z_o=(L_T/C_T)^{1/2}=(1.408nh/0.352pf)^{1/2}=63.2\Omega$$

9.2 TDR Response

A time domain reflectometer (TDR) response was simulated, using the original circuit shown in Figure 9-2, by providing an open circuit load, setting C_S to zero, and R_S equal to Z_o. Figure 9-5 shows the waveform at the output of R_S. This waveform supports the assumption that the characteristic impedance of a cell can be represented by averaging the various impedances together. The waveform rises to half amplitude and remains there for a time equal to $2t_p$. This response is indicative of a matched impedance between the source and the line.

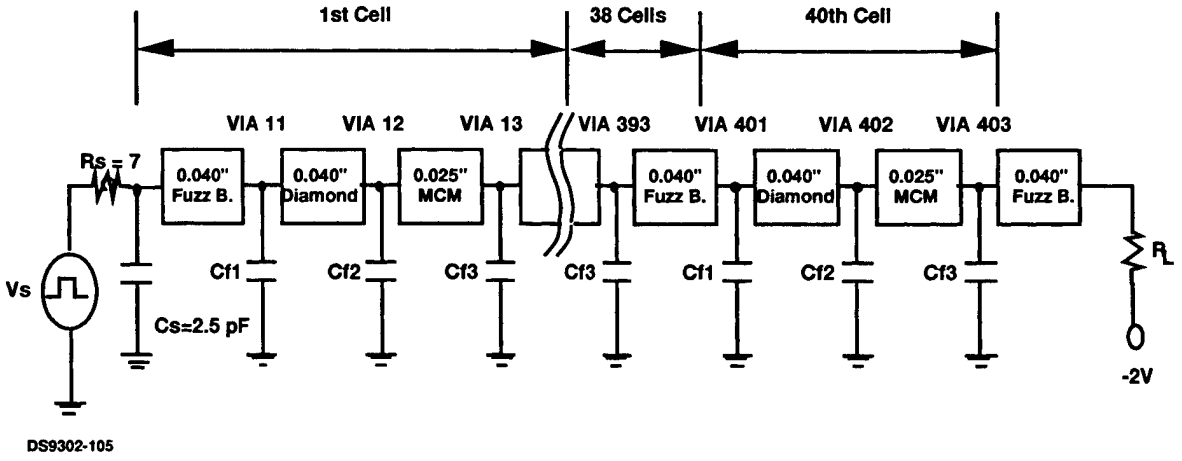


Figure 9-2. Equivalent Circuit Diagram Representing 40 Vertical Interconnect Cells

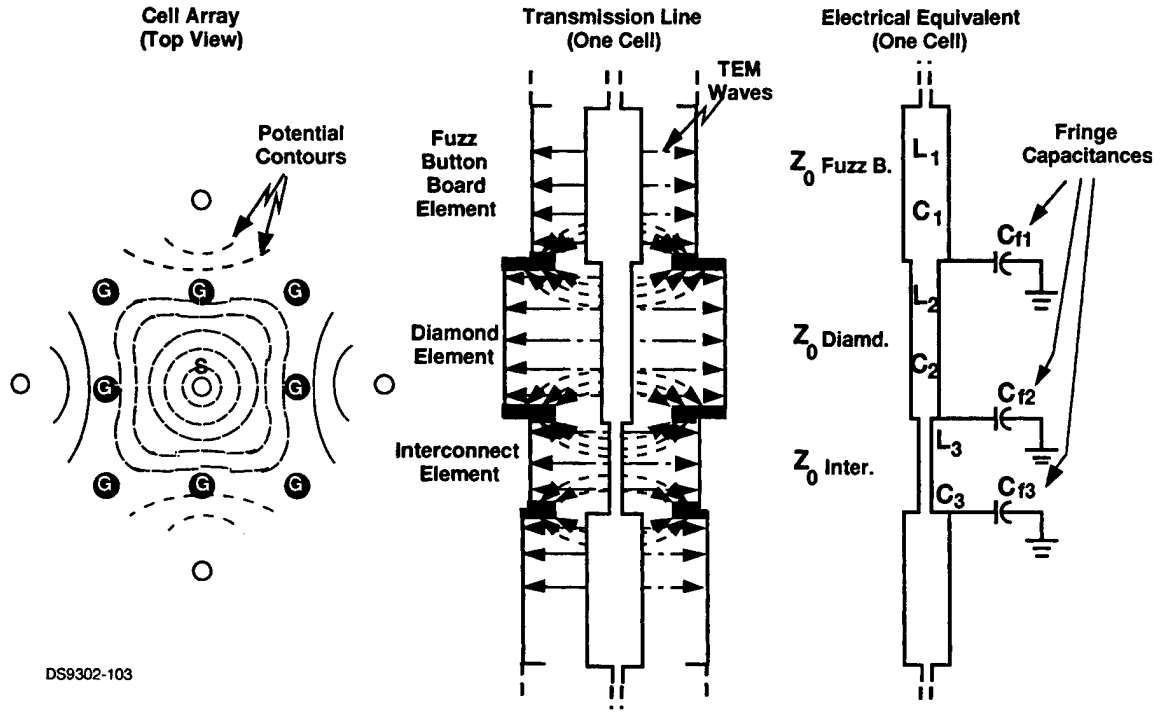


Figure 9-3. 2-D Field Solver in Cylindrical Coordinates

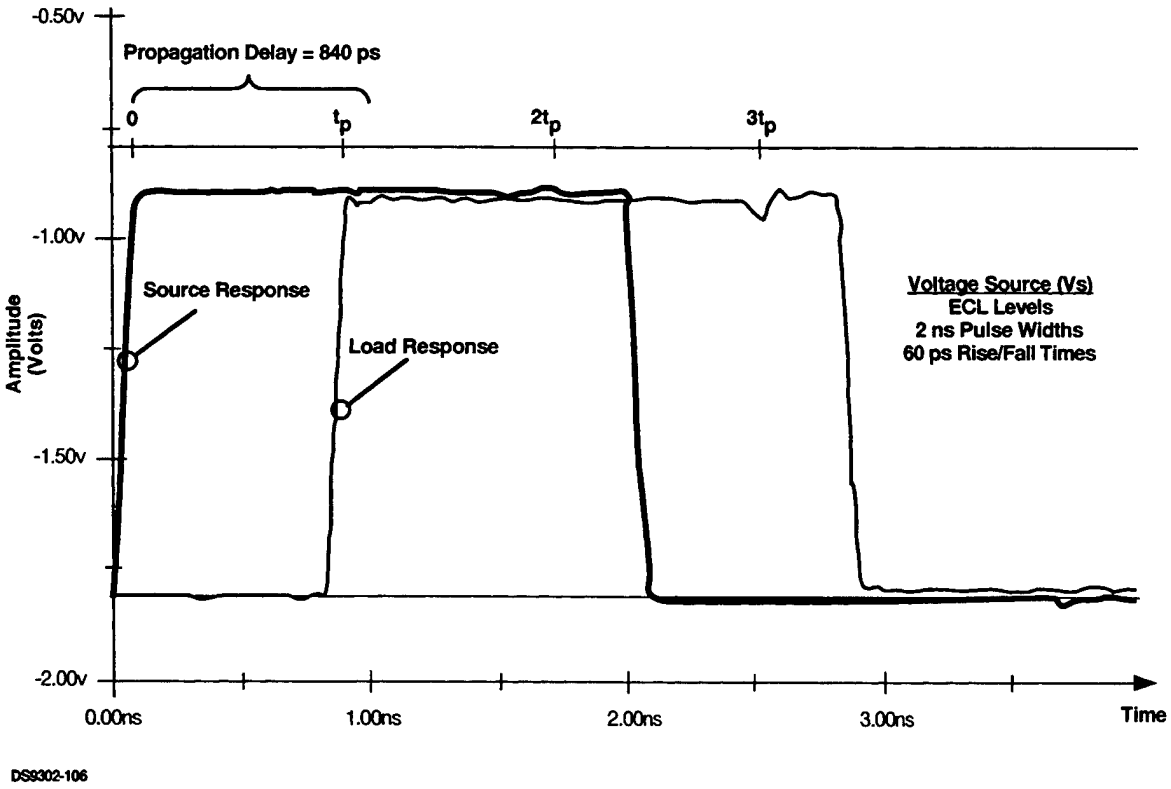


Figure 9-4. Time Domain Response for 2ns Pulse with 60ps Rise Time

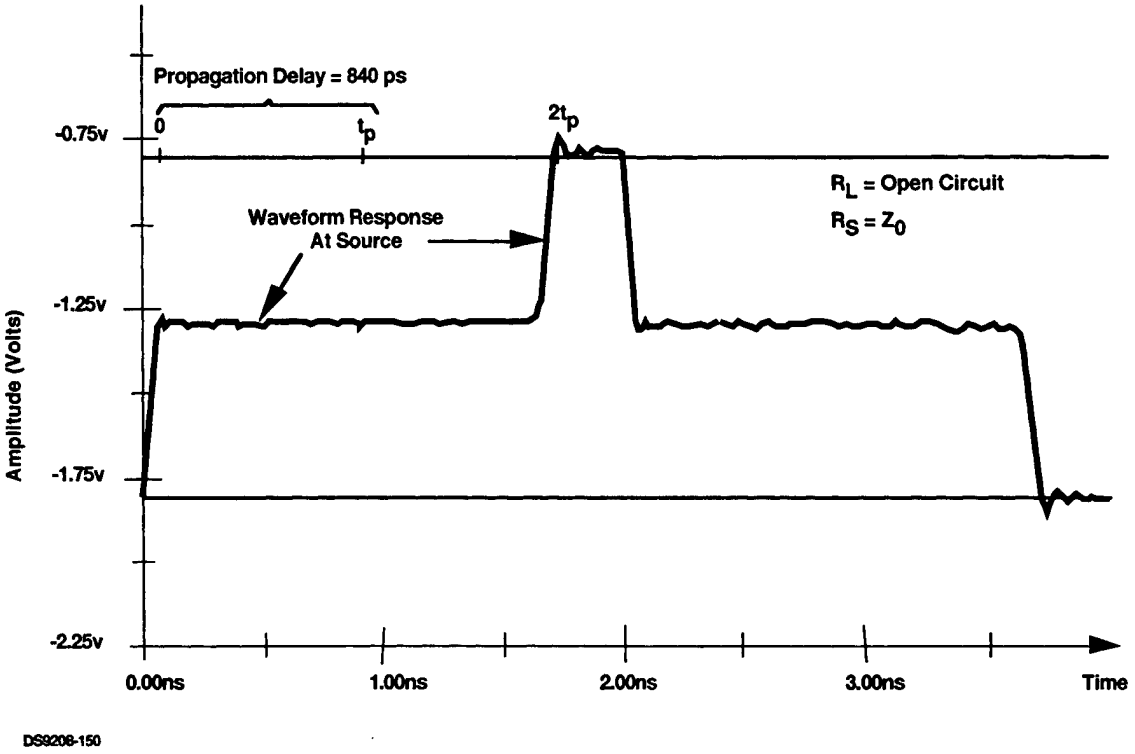


Figure 9-5. TDR Response for 40 Cell MCM Structure

It is recognized that this signal transient analysis is only a first order approximation to real world situations. However, it does justify the use of the shielded fuzz button plus vias with insulating diamond substrates as a viable structure for implementing ultra high performance 3-dimensionally interconnected packaging approaches. Adequate system bandwidth, good impedance control and minimum time delays can be adequately maintained by this concept.

9.3 Crosstalk Analysis

Figure 9-6 illustrates the equivalent circuit diagrams of a 20 cell vertical structure that was utilized for crosstalk assessments. These circuits were used for the 5x7 array of vertical cells as previously illustrated in Figure 9-1. The second circuit in this figure is used to monitor the amount of noise induced on the adjacent circuit path (i.e. "AS" in the 5x7-array diagram). The non-ideal driver used in the 40-cell baseline is also used in these 20 cell crosstalk simulations.

Figure 9-7 provides TDR response waveforms for the TDR simulations. The top left shows the response at the source. The bottom left shows the crosstalk experienced by the "AS" signal path from the "S" signal path. It shows a peak noise of about 25 mV. This is very small but this is expected since the placement of the "AS" signal path in the 5x7 array is directly behind a ground path which should provide excellent signal protection. The waveform in the top right is the signal response at the load and the bottom right waveform is the crosstalk signal zoomed out for clarity. Again, the crosstalk of 21 mV is very small. This figure also shows a calculated Zo value

of 43 Ω. Its not 50Ω but it was as close as the structure tradeoffs would allow. Notice that the TDR responses indicate a matched impedance at the 43Ω value.

The transient response and resulting crosstalk waveforms for the 5x7 array are shown in Figure 9-8.

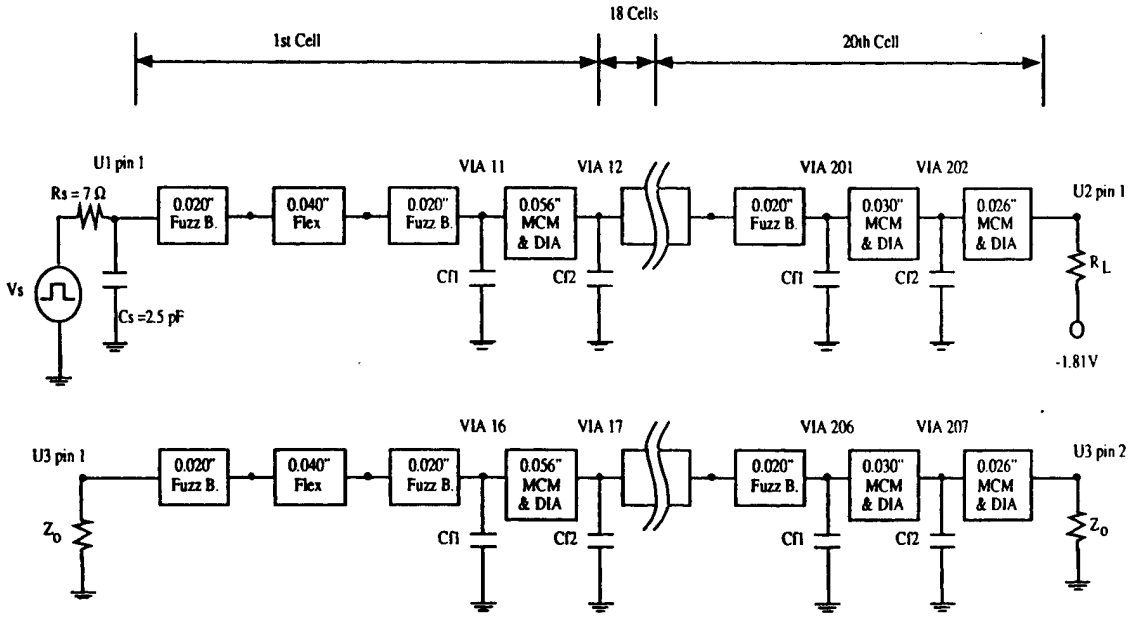


Figure 9-6. Equivalent Circuits for 20 Cell Model Crosstalk Analysis

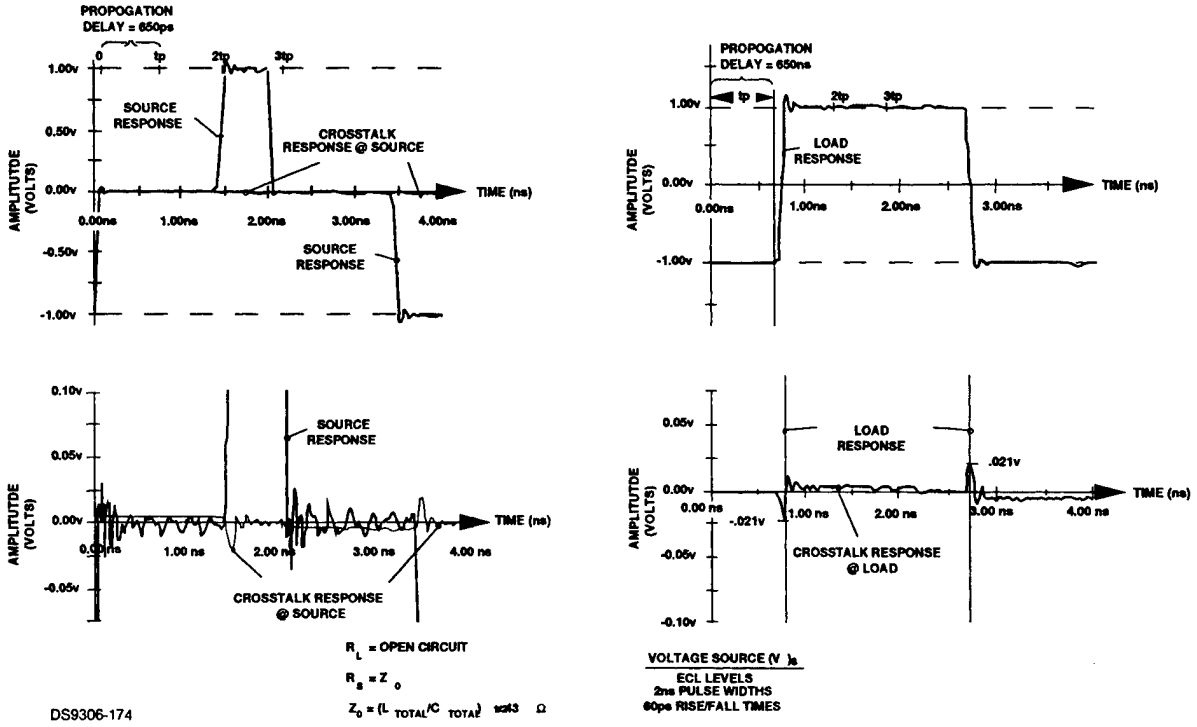


Figure 9-7. Response Waveforms for TDR and Crosstalk Analysis

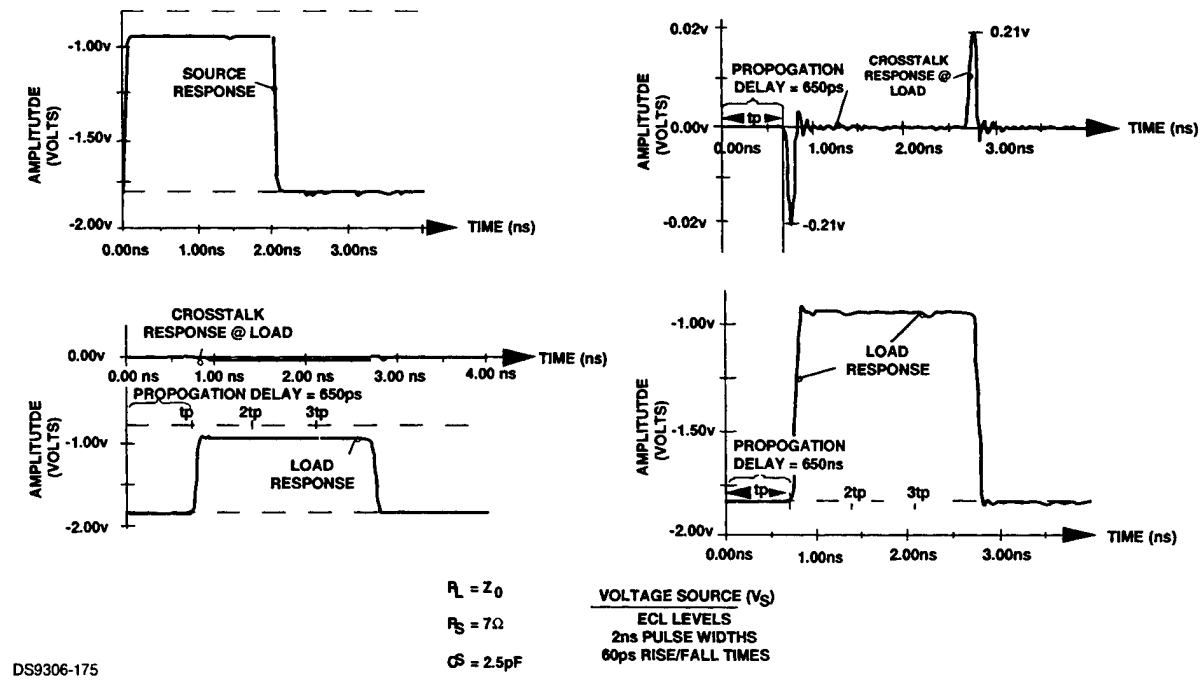


Figure 9-8. Response Waveforms for Transient Analysis of 20 Cell Structure

10. MCM THERMAL ANALYSIS AND EXPERIMENTAL RESULTS

This section provides a summary of the effort to carefully model the physical and thermal attributes of the stacked MCMs associated with the Cube Assembly in order to verify the critical thermal integrity parameters obtained from comprehensive testing of the integrated Demonstration Test Bed. This model will be compared with experimental data on:

- Thermal performance of the diamond MCM substrate
- Performance testing of the spray cooling system
- Thermal resistance testing via diode temperature monitoring

The principal unknown parameters to be evaluated by this method include the heat transfer coefficient, H, obtained at the spray-cooled diamond cooling fins at the edge of the diamond substrate MCMs, the die attach thermal resistance, $R_{th}(die)$, and the lateral thermal conductivity, k, of the diamond substrate itself. A further derived quantity is the effective thermal resistance of the spray cooling fins, $R_{th}(L_c)$, as measured by the temperature difference, T_{ref}-T_{sat}, between the base of the cooling fins and the coolant saturation temperature, T_{sat}, divided by the power into the fins.

The actual stack of boards in the 3-D MCM cube Assembly had only three diamond MCMs as indicated in Figure 10-1. Further, only four Test Characterization die (i.e., edge loop die) were powered in the demonstration testing since the corner loop die were nonfunctional. The impact of this partial functionality is shown in Figure 10-2.

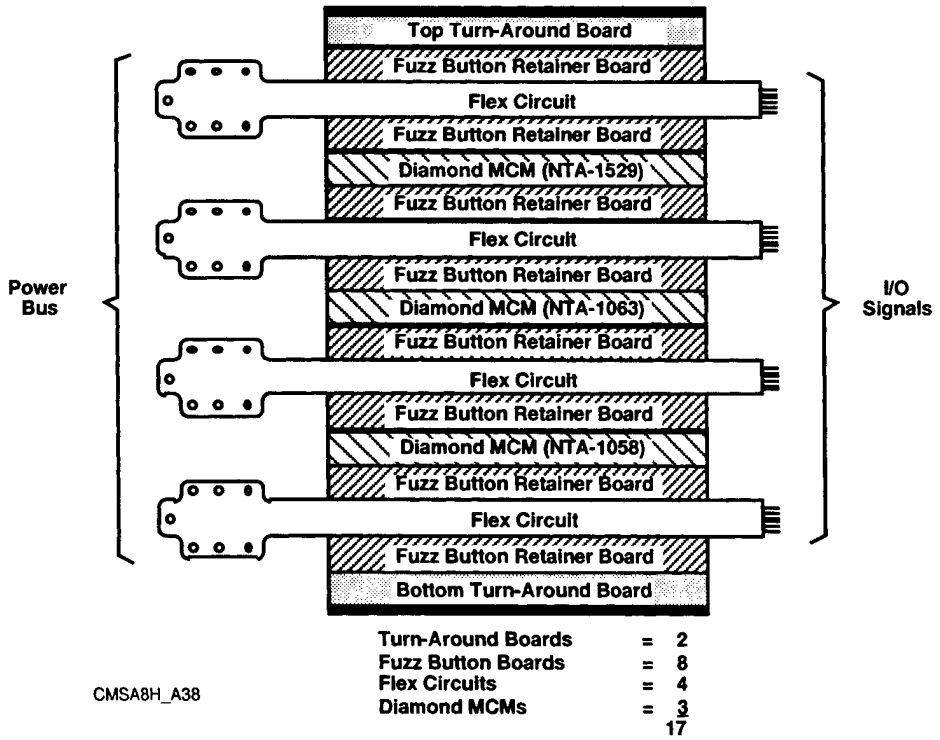


Figure 10-1. Illustration of 3-D MCM Stack in Cube Assembly

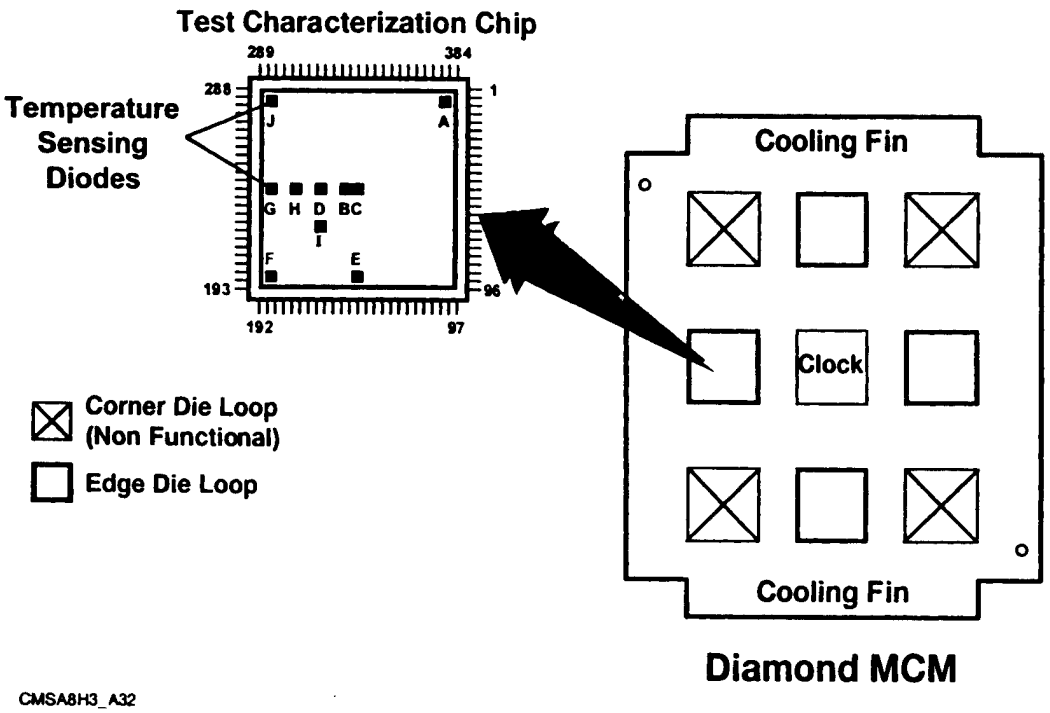


Figure 10-2. Impact of Partial MCM Functionality

The temperature sensing diodes incorporated with each Test Characterization or "ti" die were utilized to experimentally measure junction temperatures and substrate temperatures associated with each involved MCM. There are ten diodes associated with each "ti" die. Each MCM provides 80 diode differential signals that are monitored by the test and instrumentation system. All temperature measurements were extracted from the center MCM in the stack and is identified by MCM # NTA-1063. Only 26 out of a total availability of 80 diodes were functional for this testing. The plan layout of these 26 functional temperature-sensing diodes for MCM NTA-1063 is shown in Figure 10-3. Even with these partial functionality limitations, there was still a good distribution of diodes across the active area of this MCM.

Spray cooling performance was determined by monitoring the amount of power into the cooling system, the power into the 3-D cube assembly, the inlet temperature of the cooling fluid, and the temperature of the diamond cooling fin at the entry junction with the spray plate chamber.

The following thermal modeling and comparison with experimental results from the test bed are based upon the temperature measurements extracted from MCM NTA-1063. The best performance was obtained when the cube assembly was operated at a 45° angle so that gravity assistance was available to avoid flooding of the spray cooling chambers. This was because the spray manifold was designed for a stack of six diamond substrate MCMs, whereas the actual stack measured had only three diamond MCMs. Further, only four die on each MCM were powered in the measurements (plus the center clock die which was operated at lower power).

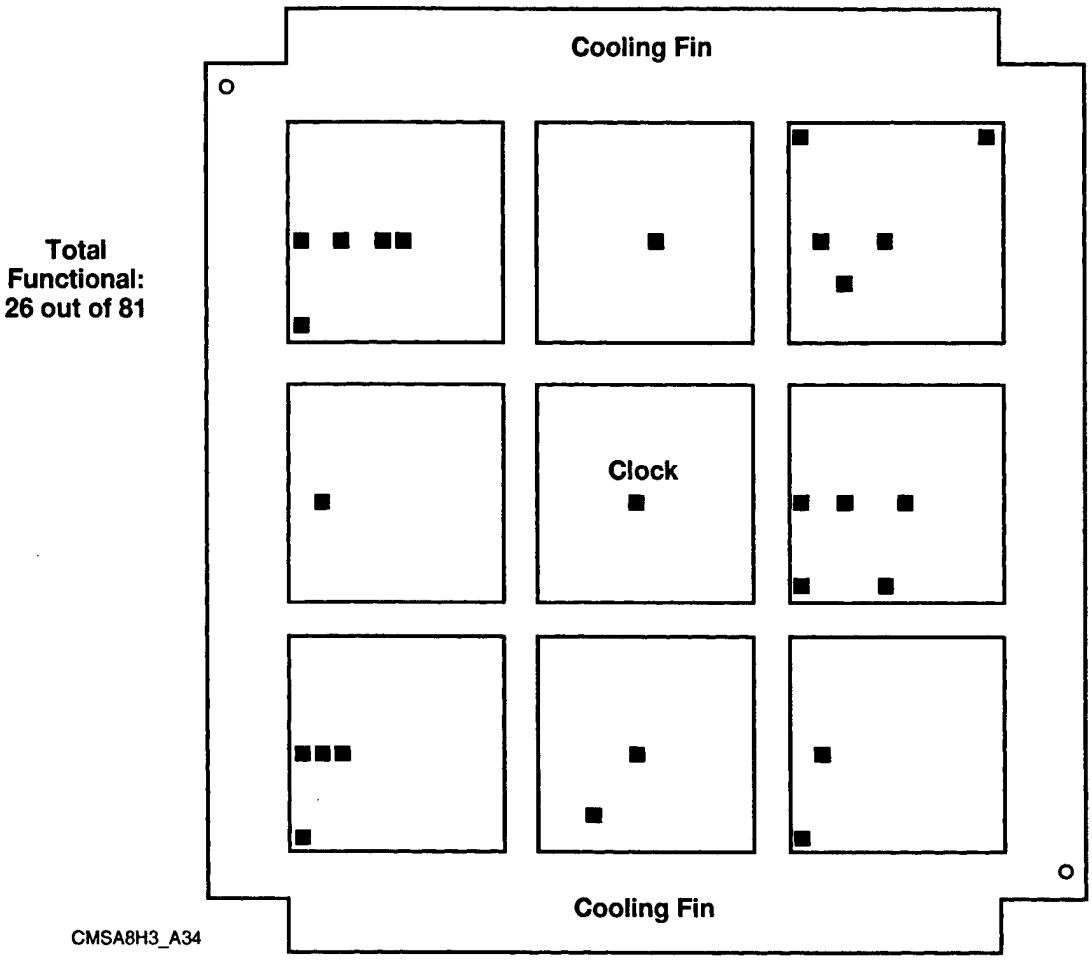


Figure 10-3. Functional Diodes for MCM NTA-1063

The effect of this is to force all of the power to pass through four (instead of eight) die-substrate thermal resistance in parallel, raising junction temperatures for any given power level. As a consequence, the maximum power level evaluated was 304 watts per MCM, instead of the 400 watts per MCM nominal design value, which meant that instead of 3x400=1200 Watts module dissipation, we had a maximum of 3x304=912 Watts, with many measurements carried out at lower power levels. Under conditions where the actual power is far below the nominal design power, the spray cooling chamber may become flooded, with a type of jet impingement cooling instead of true spray cooling. This was observed in the horizontal orientation (MCM substrates and fins horizontal) of the module, in which the excess liquid had to flow "up hill" to escape into the suction line. By tilting the MCM at a 45° angle with the suction outlets at the bottom, excellent operation was obtained with good values for the heat transfer coefficients.

10.1 Demonstration Test Plan

Table 10-1 provides an overview of the thermal testing performed on the 3-D Diamond MCM Demonstration Test Bed. Two distinct steady state thermal tests were conducted which directly support the thermal modeling and comparison results of this section. The first is identified as a "low power" test where the "ti" die were powered at the low power voltage setting of –2.7 volts.

Under this setting, the power dissipation for each of the involved MCMs in the stack is 229 watts. The second steady state test is identified as a "high power" test with a die voltage setting of –5.0 volts. The power dissipation per diamond MCM under this condition is 304 watts.

10.2 Thermal Modeling Approach

Three steps were undertaken for this thermal modeling.

1. calculating the temperature at the base of the spray-cooled heat sink fins
2. calculating (by 2-D Poisson's equation simulation) the substrate temperature rise (due to lateral thermal conduction in the diamond) between the base of the fins and the various points of interest under the IC die
3. measuring the junction to substrate temperature rise and adding it to the substrate temperature to predict die junction temperatures. These predictions are compared to the experimentally monitored temperature sensing diode points on the die associated with MCM NTA-1063.

10.2.1 Temperature at Base of Spray-Cooled Diamond Fins:

Two heat flow processes are taking place simultaneously within the spray-cooled diamond fins; lateral thermal conduction within the diamond, which leads to a temperature gradient in the fins, and heat transfer from the top and bottom surfaces of the fin from the spray cooling itself. Because this heat transfer to ambient is sensitive to the temperature difference between the fin and the saturation temperature of the fluid, T_{sat}, it is necessary to solve a differential equation to obtain the T(x) temperature distribution in the fin. At the highest power level measured (P=304 Watts per diamond MCM), the temperature rise above saturation was P $R_{th}(L_c)$ = 19.6°K, or T_{ref} = 50.6°C at the base of the spray cooling fin for T_{sat}=31.0°C. At P=229 Watts per MCM, these are P $R_{th}(L_c)$ = 14.77°K and T_{ref} = 45.77°C.

10.2.2 Temperature Distribution in Diamond MCM Substrate:

The lateral thermal conduction in the diamond MCM substrate from the powered die to the spray cooling fins leads to temperature gradients in the diamond substrate. The numerical values of temperature rise from the cooling fin base, ΔT(x,y), for the "high power" P=304 watt case (four side chips powered with 71.44 watts and the center clock chip at 18.07 watts), and for the "low power" P=229 watt case (four side chips powered with 52.72 watts and the center clock chip still at 18.07 watts) are shown in the form of a "3-D" surface graph in Figures 10-4 and 10-5, respectively. The location of the cooling fin base (at T=0) is indicated by the heavy line. The graph for the P=229 watt case shows the outline of the powered (i.e., edge loop) and unpowered (i.e., corner loop) die locations. Note that the maximum temperature rise is ΔTmax=35.71°K for P=229 watts. In addition, ΔTmax=47.41°K for the P=304 watts case.

Table 10-1. Experimental Demonstration Plan for the 3-D Diamond MCM Test Bed

1. Perform Test Bed Initiation

- Turn-on peripheral instrumentation systems
- Turn-on PC Controller
- Activate Initiation screen
- Show sequential power-up of subsystems
- Activate Fail Safe screen
- "Test" Fail Safe alarm

2. Perform "Steady State" Thermal Demo (3 MCMs/low power-2.7v)

- Activate Temperature/Diode screen
- Activate "low power" supplies
- Fill screen to "steady state" (60°C)
- Dump data to printer
- Measure input power with "Current Wand"
- Compute total power dissipation
- Annotate "ΔTs" from data print-out
- Compute cooling efficiencies
- Relate die temperatures to MCM landscape

3. Perform "Dynamic" Thermal Demo (3 MCMs/low power-2.7v)

- Dramatically slow pump rate of Spray-cooler
- Fill Screen to new "steady state" (100°C)
- Dump data to printer
- Annotate "new ΔTs" from data print-out
- Compute cooling efficiencies

4. Perform "Steady State" Thermal Demo (3 MCMs/high power-5.0v)

- Rearrange Bus Bars and Power Supplies
- Activate Temperature/Diode screen
- Activate "high power" supplies
- Fill screen to "steady state" (100°C)
- Dump data to printer
- Measure input power with "Power Wand"
- Compute total power dissipation
- Annotate "ΔTs" from data print-out
- Compute cooling efficiencies
- Relate die temperatures to MCM landscape

5. Capacity Test

- Activate Temperature/Diode screen
- Activate "high power" supplies
- Fill screen to "steady state" (100°C)
- Slowly increase heater voltage ΔV
- "Track" diode temperature rise to 135° C
- Immediately "Power Down" system
- "Track" diode temperature fall to ambient conditions

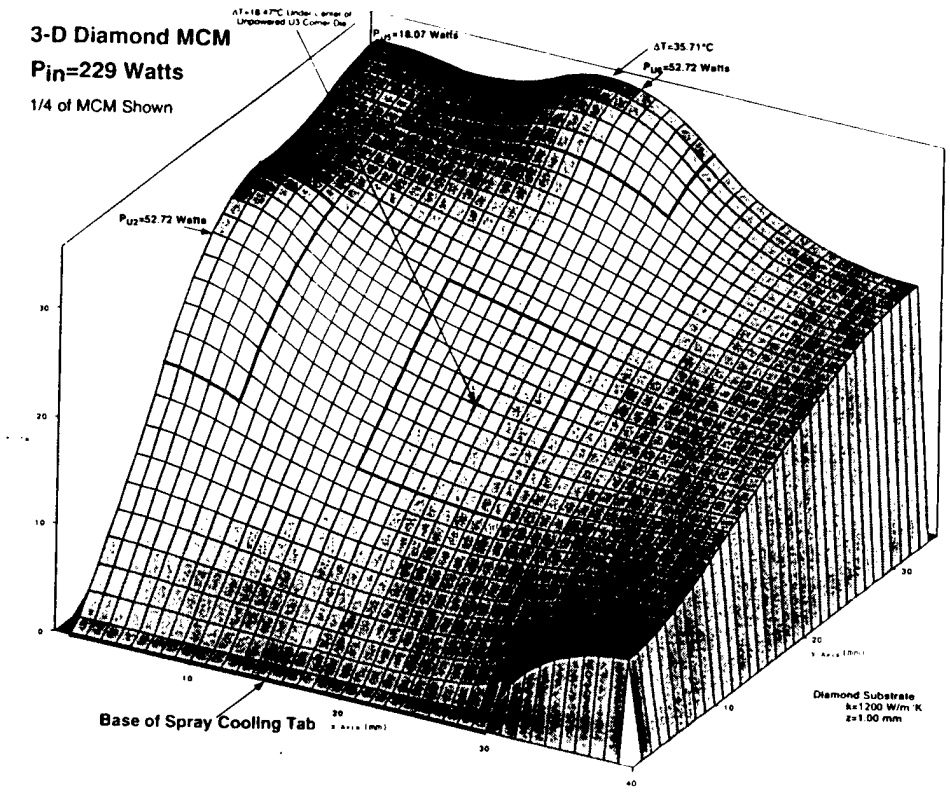


Figure 10-4. Temperature Distribution in Diamond MCM (Low Power Case)

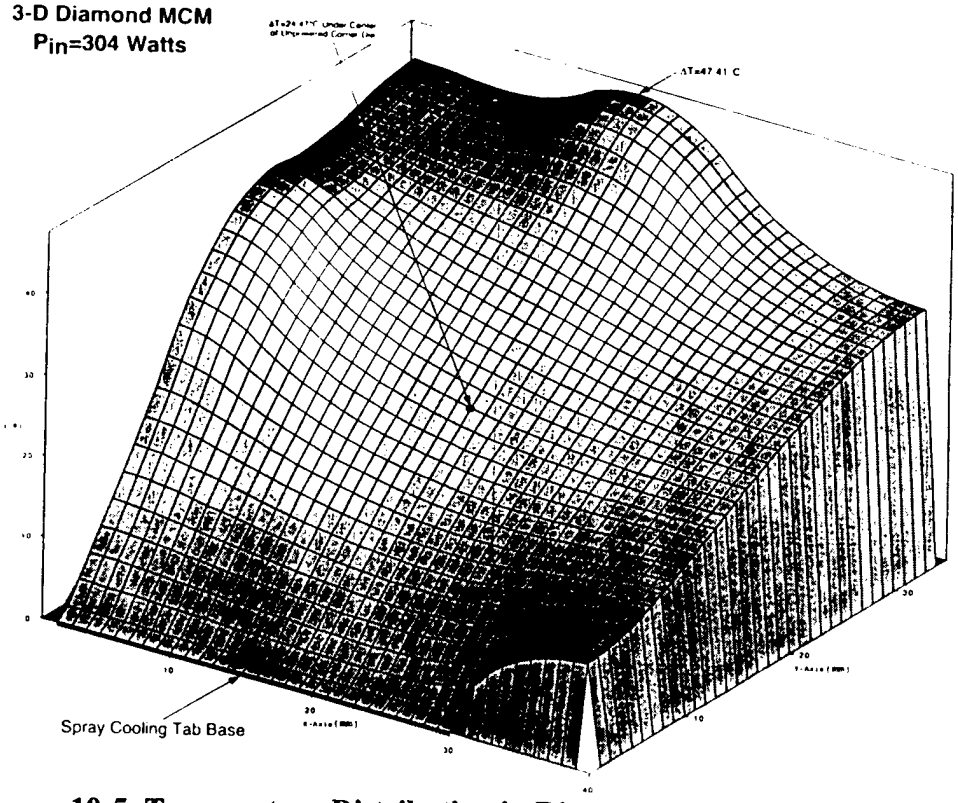


Figure 10-5. Temperature Distribution in Diamond MCM (High Power Case)

10.2.3 Calculation of IC Junction Temperatures

In both the 2-D Poisson's Equation simulation of $\Delta T(x,y)$ and in the calculation of the difference in temperature between the die junction temperatures and the diamond substrate temperature underneath, it is assumed that the power dissipation is uniform over any given IC chip. It is also assumed that all IC chips have the same die attach thermal resistance, $R_{th}(die)$. Hence the absolute junction temperature at any point on an IC die will be given from

$$T_j(x,y) = T_{ref} + \Delta T(x,y) + P_{IC}\, R_{th}(die)$$

Where T_{ref} is the previously calculated temperature at the base of the spray cooling fin, $\Delta T(x,y)$ is from the 2-D thermal spreading calculation results, and the junction to substrate temperature rise is calculated for each chip based on its power dissipation, P_{IC}.

Adjustment of the three critical parameters (H, $R_{th}(die)$ and k) to obtain the best overall fit of the experimental temperature data for the two cases involves physical insight. The goal was to get good overall agreement. An Excel worksheet was used to select these critical parameter values and determine the best fit. For example, for the P=229 watt case at the center of the unpowered die, T_j=64.24°C was calculated vs. 64.89°C measured. For the 304 watt case it was 70.24°C calculated vs. 73.54°C measured. In the 304 watt case the clock die was calculated at T_j=99.68°C, but measured at 96.06°C and 100.75°C in two measurements only about a minute apart. Most of the measurements are within about ±4°C of the calculated values. One particular diode consistently gave values around 10-12°C lower than expected (which might well be an experimental problem with this diode). In general, the quality of fit to the experimental temperature data is very good.

10.2.4 Heat Transfer Coefficient

The best-fit heat transfer coefficient value obtained from this work was H=1.15 W/cm2°K (or 2018 BTU/HrFt2°F) with the FC87 (or FC5070) (T_{sat}=31°C nominal) Fluorinert fluid supplied by ISR with the cooling system. This value seems very good for a geometry in which the angle between the spray and most of the sprayed diamond tab surface is quite low. At this H, the effective thermal resistance of the 2.32-inch wide by 0.306-inch long spray-cooled fins (from fin base to T_{sat}) was 0.129°K/Watt for each tab (0.0645 °K/W for the two tabs on each diamond MCM). Hence, at P=304 watts, the base of the spray-cooled diamond tabs was only T_{ref}-T_{sat} =19.6 °K above the fluid saturation temperature. The best fit value for lateral thermal conductivity of the z=1.00 millimeter thick diamond substrate material was found to be k=1200 W/m°K. This is in excellent agreement with the values claimed by Norton Diamond Film for this material. Note that this k value has been obtained after the 7200 via holes were drilled in the substrate and all metallization and MCM processing was completed. This experimental verification should eliminate concerns that drilling and processing might seriously degrade the thermal performance of the diamond substrate material

10.2.5 Die-to-Substrate Thermal Resistance

The final critical thermal parameter evaluated was the die to substrate thermal resistance, R_{th}(die). The best-fit value obtained for this parameter was R_{th}(die) =0.55 °K/Watt. This is a rather high value for a 1cm x 1cm chip in a thermally sensitive application. For example, at the "high power" case of P=304 watts per MCM, the junction-to-substrate temperature had a rise of 39.3°K. The total temperature rise due to lateral heat flow through the z=1.0 millimeter thick diamond substrate over the 33 millimeter path from the cooling fin base to the hottest point on the MCM is only 47 °K. This means that nearly 40 °K is wasted in die attach thermal resistance. There is every reason to believe, however, that this could be greatly improved by optimizing the die attach technology. Other than the higher than desired R_{th}(die) values, the thermal results measured for the 3-D diamond MCM cube assembly built in this program were very gratifying, and a clear demonstration of the viability of this 3-D diamond MCM concept.

APPENDIX A

The Role of Diamond Substrates in 3-D MCMs

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THE ROLE OF DIAMOND SUBSTRATES IN MCMs

by

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Introduction

Assuming that its cost can be brought low enough, diamond offers a promising solution to many difficult electronic packaging problems. For example, the multi-chip module (MCM) approach for achieving very high chip packaging densities is of particular interest for high performance, high clock rate digital systems, where signal latency due to excessive inter-chip interconnect line lengths can prove a major limitation. As IC chips are operated at higher frequencies, their power dissipations tend to increase proportionately. As these chips are jammed together very closely in MCM packaging, the power density levels get very high indeed. These severe thermal management problems represent a serious barrier to the application of MCM technology in high performance systems. Diamond, which has the highest thermal conductivity known, has been used as a heat sink material in critical device applications for many years. Only recently has the promise of major reductions in the price of diamond allowed its consideration for use in electronic thermal management applications such as MCMs. The combination of high thermal conductivity with an electrically insulating nature (which allows the easy fabrication of isolated signal interconnects), makes diamond an ideal packaging and MCM substrate material [1].

Comparison of Diamond with Conventional Packaging Materials

In many ways diamond offers virtually an ideal material for electronic packaging applications, including MCM substrates. Of prime interest is its extremely high thermal conductivity, about k=2000 W/m°C in natural diamond, with comparable values measured in chemical vapor deposition (CVD) synthetic diamond [2]. Table 1 compares the thermal conductivity of diamond with those of various other electronic packaging materials. Included in Table 1 are the coefficient of thermal expansion (CTE) values and note of the electrically conducting or insulating nature of the materials.

Table 1. Electronic Packaging Materials Comparison

Material	Thermal Conductivity W/m°C	Electrical Insulator? Y/N	Thermal Expansion ppm/°C
Diamond:			
Natural	2000	Y	0.8-1
CVD	700-1700	Y	1-1.5
Beryllia, BeO	220	Y	6.4
AlN	70-230	Y	3.3
Alumina, 99%	29	Y	6.3
GaAs	45	Semi	5.9
Silicon	149	N	2.6
Kovar® (FeNiCo)	17	N	5.9
Molybdenum	146	N	5.1
Aluminum	237	N	23.8
Copper	396	N	16.8
Silver	28	N	19.6
Diamond-Epoxy	8.7	Y	120
Silver-Epoxy	5.8	N	120
Polyimide	0.2	Y	>50

As can be seen from Table 1, the metals silver and copper are the only materials to come within a factor of 5 of the thermal conductivity of diamond, but they are not insulators and have CTE's much higher than that of silicon. Silicon itself

can be used as an inexpensive MCM substrate material (with ideal CTE match, of course), but it is not an insulator and its thermal conductivity (149 W/m°C) is only a little better than that of molybdenum, and no match to that of diamond. Most insulators tend to have poor thermal conductivities; only beryllia and aluminum nitride come within an order of magnitude of diamond. We see that diamond, provided it can be manufactured in volume and sold at an acceptable price, is truly favored by nature as an ideal electronic packaging material.

Application of Diamond for Conventional 2-D Packaging

The majority of MCM's and other electronic packages currently fabricated are of the conventional 2-dimensional configuration, in which all of the IC die lie in a single plane (generally packed as closely together as their substantial chip areas and the inter-chip interconnect technology will allow). The selection of substrate material for conventional 2-dimensional packages or MCMs is generally balanced between consideration of thermal expansion coefficient match (for which silicon is ideal), manufacturability, and cost (for which alumina is often used), and thermal performance (which often necessitates backing with copper or employing other heat sink methods). While forced-air or other heat exchange approaches are often adequate to cope with the average power density on 2-D MCMs, a frequent problem is that of "hot spots", or single chips operating at much higher than average power levels. Due to inadequate lateral thermal conductivity in the substrate material, these hot spots may degrade the chip reliability substantially. This case may be quantitatively illustrated by considering a circular geometry (chosen for ease in analytical solution) with a uniform power dissipation over a chip of radius R_i centered in a substrate of radius R_o with a heat sink at temperature T_o at its outer edge, assuming heat transfer only through thermal conduction in the substrate. Solving the heat flow differential equation (Poisson's equation) for this cylindrical geometry is straightforward, giving the maximum temperature (at the center of the chip), T_m, versus total chip power, P, as [1]:

$$T_m - T_o = (P/2\pi kz)\,[\ln(R_o/R_i)+1/2] \qquad (1)$$

where k is the substrate thermal conductivity and z its thickness, and T_m-T_o is the maximum temperature rise above the heat sink temperature. Note that the assumption here is that the power, P, is uniformly distributed over the chip area, there are no other (e.g., convection or radiation) heat transfer mechanisms operative, and that the lateral thermal conductivity of the die is negligible in comparison to the substrate.

As a specific example, consider the case of a $2R_i$=1cm diameter chip dissipating P=20 watts at the center of a $2R_o$=10cm (4") diameter substrate, z=1mm thick, edge cooled at T_o=300°K (26.84°C). If the substrate were silicon (k=149 W/m°C), the temperature at the center of the die, T_m, would be 60°C above T_o. Operation of the IC at this higher junction temperature would degrade the reliability or serious reduction in MTBF. On the other hand, using k=2000 W/m°C diamond would give only a T_m-T_o=4.46°C temperature rise and a negligible degradation in MTBF. This particular example with diamond is graphically illustrated in Figure 1.

The use of more normal substrate materials such as alumina would give catastrophic T_m-T_o = 253°C to 407°C temperature rises. Such materials are usable only where the heat flow through the substrate is essentially normal to the substrate plane, or removed directly from the die by other means.

Potential For 3-Dimensional Interconnects

There are enormous advantages in going to 3-dimensionally interconnected packaging approaches, as opposed to the edge-connected 2-D modules usually used. These involve both reducing the maximum electromagnetic propagation delay, and in drastically reducing the critical path delays for signals among smaller groups of chips implementing key functions. For example, in a vector-pipelined processor machine whose goal is to complete one floating point operation in each processor in each nanosecond, a straight Z-axis interconnect between the processor logic chips on each neighboring board may be the only way to achieve this minimum propagation delay.

In 3-dimensional MCM packaging, use is made of the fact that IC chips are thin (typically 0.6mm or less), permitting very high volume density packaging. Figure 2 dramatically illustrates how, whereas a given die has only 8 nearest neighbors in 2-D, in 3-D (assuming a 1.5 cm X-Y pitch and a 2.5 mm Z pitch) 116 die may be reached with essentially the same signal interconnect length. For example, if the interconnect delay is 150 ps/inch, and the VLSI chips have 10,000 gates,

then the 3-D geometry of Figure 2 places over a million gates within 650 ps worst case delay time. If these 117 chips had to be spread out horizontally, the worst-case delay between chips would exceed 1.7ns, which would represent a significant performance compromise for system clock rates above the 50 MHz to 100 MHz range, and virtually preclude operation at rates above 250 MHz to 350 MHz if full corner-to-corner propagation is required within the cycle. With 3-D packaging, this is extended to nearly 1 GHz, a major improvement.

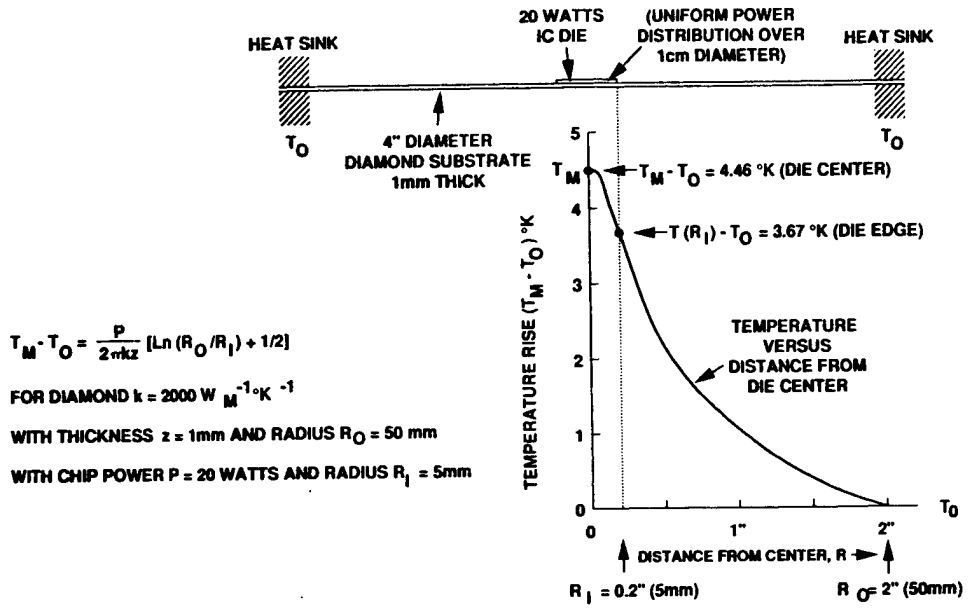

Figure 1. Diamond's Ability for Reducting "Hot Spot" Temperature Rise

Application of Diamond for 3-D Packaging

There are two key problems involved in implementing 3-D packaging, both of which diamond can help solve: 1) achieving the vertical interconnects between boards with high density in a practical, demountable, reworkable fashion, and 2) getting the heat out of the "cube" (the completed 3-D interconnected system) due to the substantial power dissipation from all of the high speed IC's operating in a small volume.

A very practical method for distributing close vertical interconnects over the full area of the boards is shown in cross section by Figure 3. Conductive "fuzz buttons" (rather like subminiature gold-plated Brillo ® pads) are stuck in arrays of holes in a plastic spacer board that is placed between the diamond MCM boards to be vertically interconnected. The fuzz buttons, typically 0.020 in diameter, extend beyond both sides of the spacer board by 0.004" or so, so that they make solid contact to the pads on the boards above and below the button board or spacer board when the mating force used in assembly is applied. This precision plastic spacer board (approximately 0.04" or 40 mils in thickness) has spacer holes for the IC die, and a large number of 20 mil diameter holes into which the fuzz buttons are forced (currently commercially available in diameters as small as 0.020'). Random contacts under compressive forces give the fuzz button a self cleaning property as well as high current carrying capacity. This form of vertical spacer in a 3-D structure offers low inductance and resistance paths, as well as application flexibility, durability, and repairability by elimination of soldered and wire-bonded contacts.

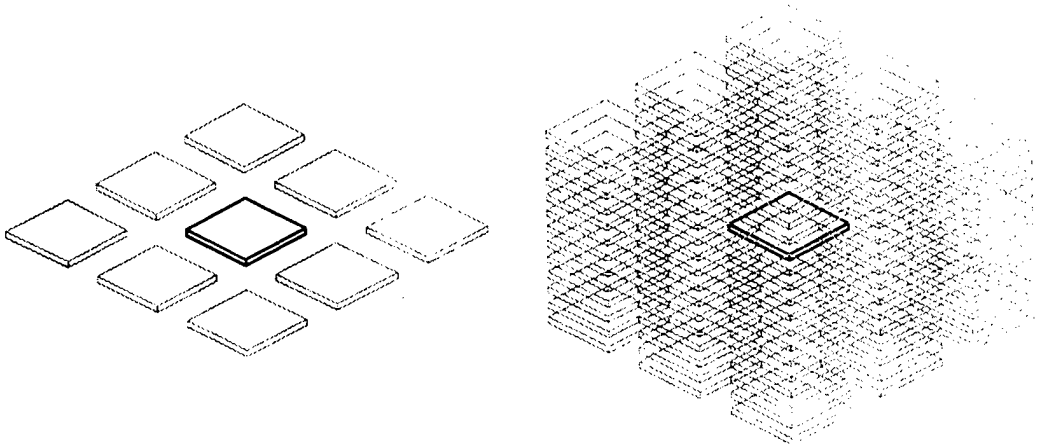

Figure 2. Comparison of 2-D and 3-D MCM Signal Interconnect Lengths

Notice from Figure 3 that the technique for passing signals vertically through the insulating diamond substrates themselves is by metal filled holes (called VIAs) having the same center to center location geometry as the fuzz buttons on the spacer board. If it is assumed that these fuzz buttons and VIAs can be placed in a diagonal square array with horizontal and vertical center to center pitch of 40 mils, there is room for up to 9765 vertical interconnect channels in a 4" square spacer board or diamond substrate even after the die clearance holes are accounted for. Considering that the high density multi-layer horizontal interconnect system can be interspersed between each layer of fuzz button contacts, this should be far more vertical interconnect channels than needed in most real systems.

Thermal Considerations for 3-D Packaging

Methods of implementing, conveniently and practically, high density arrays of vertical interconnects between adjacent boards exist as demonstrated in previous Figure 3 but suffer the disadvantage that they block the inter-board spaces through which cooling fluid (such as air, or possibly a liquid such as Fluorinert ®) would ordinarily be passed.

This difficulty of extracting heat convectively from such a 3-D interconnected MCM package ("cube computer") can be solved by using an electrically insulating, super high thermal conductivity substrate material like diamond to simply conduct the heat out laterally through the substrate to heat sinks at opposing faces. As illustrated in Figure 4, consider a stack of boards, each populated with a high density of equal power dissipation chips. This case represents essentially a uniform average power density, P/A, due to chip dissipation over the substrate.

Solving the one-dimensional (x in Figure 4) heat flow problem with a uniform applied power density flowing into the heat sinks at temperature T_0 at x = o and x = L gives a parabolic temperature distribution across the substrate with maximum temperature, T_m, at the center, x = L/2, of

$$T_m - T_o = \frac{1}{8}\left(\frac{P}{A}\right)\frac{L^2}{kz} \qquad (2)$$

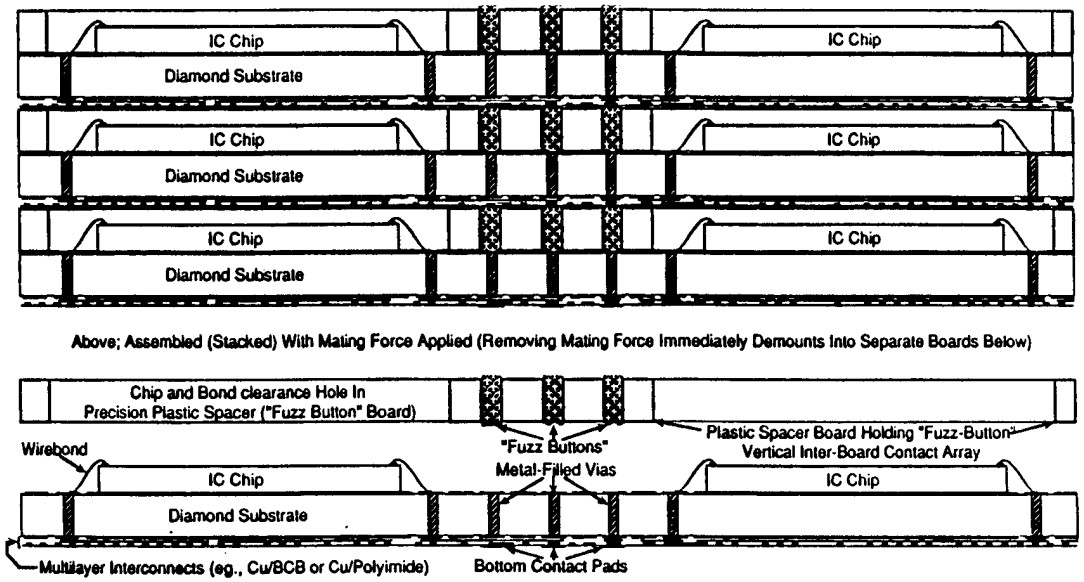

Figure 3. Cross Section of 3-D Diamond MCM Assembly

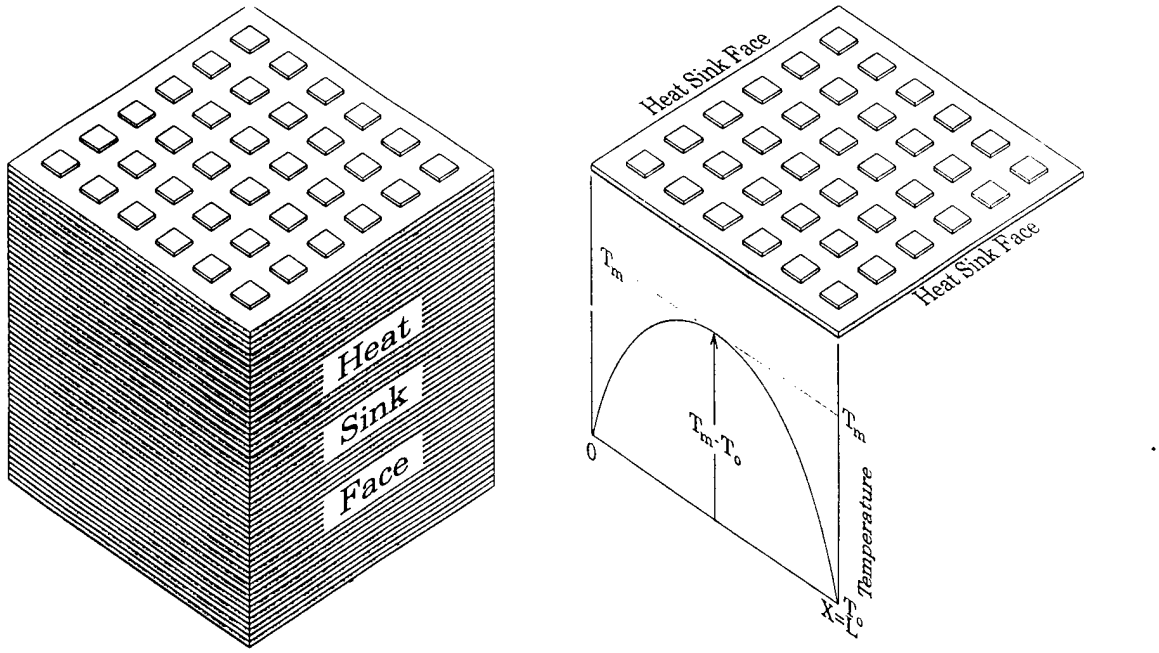

Figure 4. 3-D Diamond MCM System Conductively Cooled through two Opposing Faces

where, as usual, k is the thermal conductivity and z the thickness of the substrate, and L the spacing between the two heat sink faces (substrate edges). If the width of the substrate (length of the heat sink face) is W, then the area is given by A=LW, and the thermal resistance of the substrate is

$$R_{th} = \frac{T_m - T_o}{P} = \left(\frac{1}{8kz}\right)\left(\frac{L}{W}\right) \quad (3)$$

For the particular case of a square substrate, L = W and the thermal resistance is just

$$R_{th} = \frac{1}{8kz} \quad (4)$$

again assuming conductive cooling through two opposing edges (cube heat sink faces) of the square substrate.

For example, as shown in Figure 4, consider the case of 100mm (4") square diamond substrate 1mm thick. From Eq. (4) with k=2000 W/m°K and z = 0.001m, we have R_{th} = 0.0625°K/W (62.5°K/kilowatt), a remarkably small thermal resistance. If the total board dissipation were 500 watts, the temperature rise would be a maximum of only 31.25°K. For a 40-board system (100mm cube), the thermal resistance is only 1.56°K/kilowatt, or a power handling capacity of 20,000 watts for a modest 31.25°K temperature rise above the heat sink temperature.

Signal Integrity Assessment for the 3-D Interconnect Structure

The task every designer faces in high speed interconnects is in guaranteeing that signals are propagated between ICs throughout the 3-D MCM assembly with acceptable (minimum) levels of distortion. Ultra high performance for the 40 board system (100mm cube) shown in previous Figure 4 means ECL signal levels operating up to 1GHz clock speeds, having 60 ps rise and fall times.

Given the signal demands outlined above, the vertical interconnect structure must be thought of in terms of a "propagation medium," utilizing the concept of characteristic complex impedance, signal bandwidth, and time delay as frequently employed in microwave design. These vertical interconnects must be treated as a transmission line, characterized by its impedance, loss, and electrical length. The impedance of the signal sources and signal loads must also be considered. In general this network can be modeled by distributed resistance, inductance, and capacitive elements.

A time domain transient analysis was performed to determine characteristic impedance, signal bandwidth, and time delay for one complete top to bottom interconnect path thru all 40 MCM diamond substrates and spacer boards stacked vertically in the cube computer concept. This simulation analysis was performed using the XFX® and XNS® analysis software from Quad Design Technology, Inc. [4].

The transmission line parameters of each physical cell or vertical line segment were first determined using the 2-D field solver XFX®. The physical model for one vertical cell is shown in Figure 5. Each cell contains three elements: 1) a fuzz button ~~spacer~~ board, 2) a diamond substrate, and 3) an x and y axis interconnect layer. A 5 x 7 diagonal square array of these cells was also input to the field model to represent a signal isolation pattern for these vertical interconnect structures. Notice in Figure 5 that a signal was assigned to one of the center cells and the remaining 34 were grounded. The alternate signal (AS) conductor can be utilized by the field model to assess crosstalk but was not addressed by this paper. The fuzz buttons and metal filled VIAs had diameters of 20 mils and 4 mils, respectively. Three separate runs were performed with the field solver, one for each element, to generate the transmission line parameters per unit length. Table 2 presents these resulting parameter values. These parameters include inductance (L) and capacitance (C) per inch, dc resistance (Rdc) and skin effect (R_{skin}) resistances, and its characteristic impedance (Z_o).

The circuit diagram shown in Figure 6 was input into XNS® to perform the transient analysis of a signal vertically transmitted through 40 MCM cells stacked on top of each other. The ideal voltage source (V_s) drives ECL levels with 60 ps rise and fall times and a pulse duration of 2 ns. The source resistance (R_s) and capacitance (C_s) values simulate the output characteristics of a true ECL driver. Each box represents an MCM element in the signal path and states the appropriate lengths of each segment. The lumped capacitances, C_{f1}, C_{f2}, and C_{f3}, represent the fringe capacitances at the line segment

interfaces. These fringe capacitances were calculated with a 2-D field solver in cylindrical coordinates using a custom software package [5]. The load resistance (R_L) provides a matched impedance load. This circuit assumes an ideal ground return path and does account for skin effect and dc resistances. The calculated fringe capacitances caused by the non uniform geometries at each element interface (conductors passing through ground planes) are tabulated in Table 3.

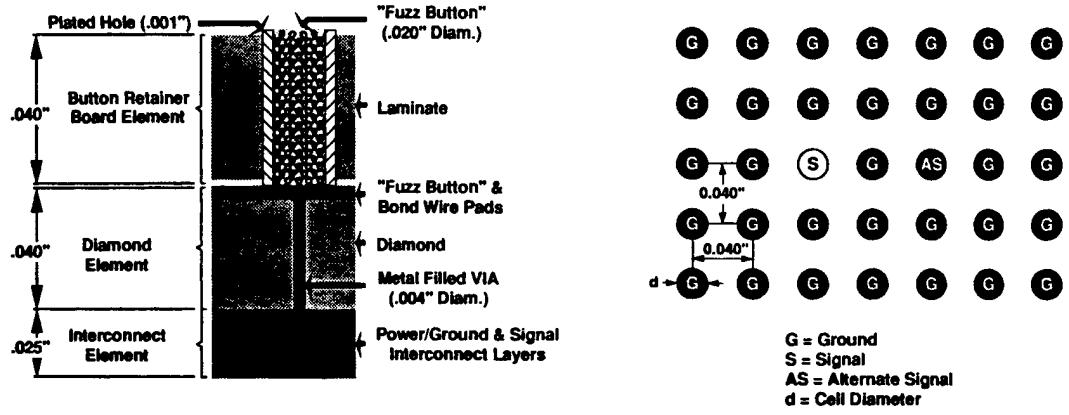

Figure 5. Vertical Interconnect Model used in Field Solver

Table 2. Transmission Line Parameters for One Cell

3D MCM Element	Dielectric Constant	L (nh/in)	C (pf/in)	Z_0 (Ω)	R_{skin} (Ω-ns^.5)	Rdc (Ω)
Fuzz Button Board	3.1	6.069	3.667	40.68	0 083	0.002
Diamond Layer	5.6	16.322	2.463	81.41	0.302	0.073
Interconnect Layer	3.5	16.322	1.539	102.98	0.302	0.073

These fringe capacitances and other transmission line parameters for the equivalent 40 cell circuit were input to XNS® to simulate a transient response. Figure 7 illustrates the waveforms of the 2ns pulse at both the source and load positions. Notice that the 60ps rise time is preserved indicating adequate signal bandwidth for this vertical interconnect structure. The propagation delay (t_p) through the 40 cells is approximately 840ps.

A time domain reflectometer (TDR) response was simulated, using the original circuit shown in Figure 6, by providing an open circuit load, setting C_S to zero, and R_S equal to Z_0. Figure 8 shows the waveform at the output of R_S. This wave form supports the assumption that the characteristic impedance of a cell can be represented by averaging the various impedances together. The wave form rises to half amplitude and remains there for a time equal to $2t_p$. This response is indicative of a matched impedance between the source and the line.

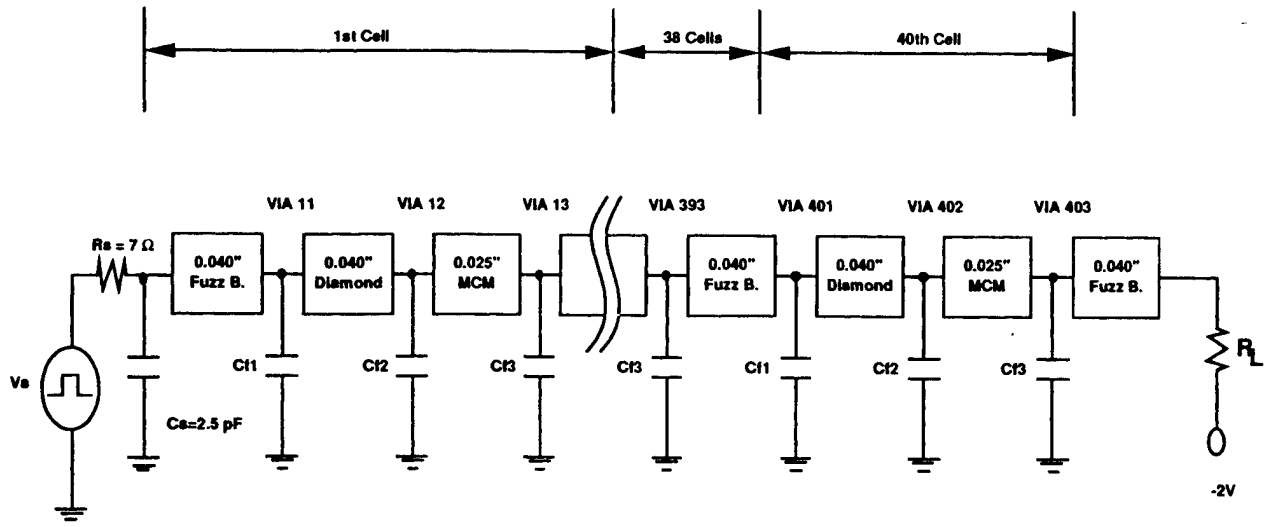

Figure 6. Equivalent Circuit Diagram Representing 40 Vertical Interconnect Cells

Table 3. Element Interface Fringe Capacitances (One Cell)

Element Interface	Term Definition	C (pf)
Fuzz Button - to - Diamond	Cf1	0.028
Diamond - to - Interconnect	Cf2	0.008
Interconnect - to - Fuzz Button	Cf3	0.025

Summary

While the enormous increases in integrated circuit speeds realized over recent years offers the possibility of major enhancements of digital system speeds, the fast signal risetimes and high power levels of these chips lead to formidable packaging challenges in trying to achieve these enhanced speeds at the system level. The extremely high conductivity of diamond, coupled with its electrically insulating nature and very low thermal expansion, make it an ideal choice for solving many of these packaging problems. In fact, the thermal conductivity is so high as to allow many hundreds of watts to be extracted from a 1mm thick diamond substrate by lateral thermal conduction alone.

What the diamond does is to laterally conduct the heat generated by the logic out of the "battle zone" of the actively populated cube itself. This frees the designer to fully utilize all of the space between boards to implement a high area density array of vertical interconnects between all adjacent boards in the stack to minimize interconnect delays. Because there is no need to co-utilize this inter-board space to meet cooling requirements, the designer can make use of the most reliable, simple, cost effective, demountable, etc., vertical inter-connect methods available.

The various key components of the vertical interconnect structure have been identified and include commercially available fuzz buttons in spacer boards married with metal filled VIAs in the insulating diamond substrates. Using transmission line integrity assessment tools, it is seen that this structure provides adequate signal bandwidth and controlled impedance for minimum distortion propagation of ECL-like digital signals having clock speeds approaching 1GHz with 60 ps rise and fall times.

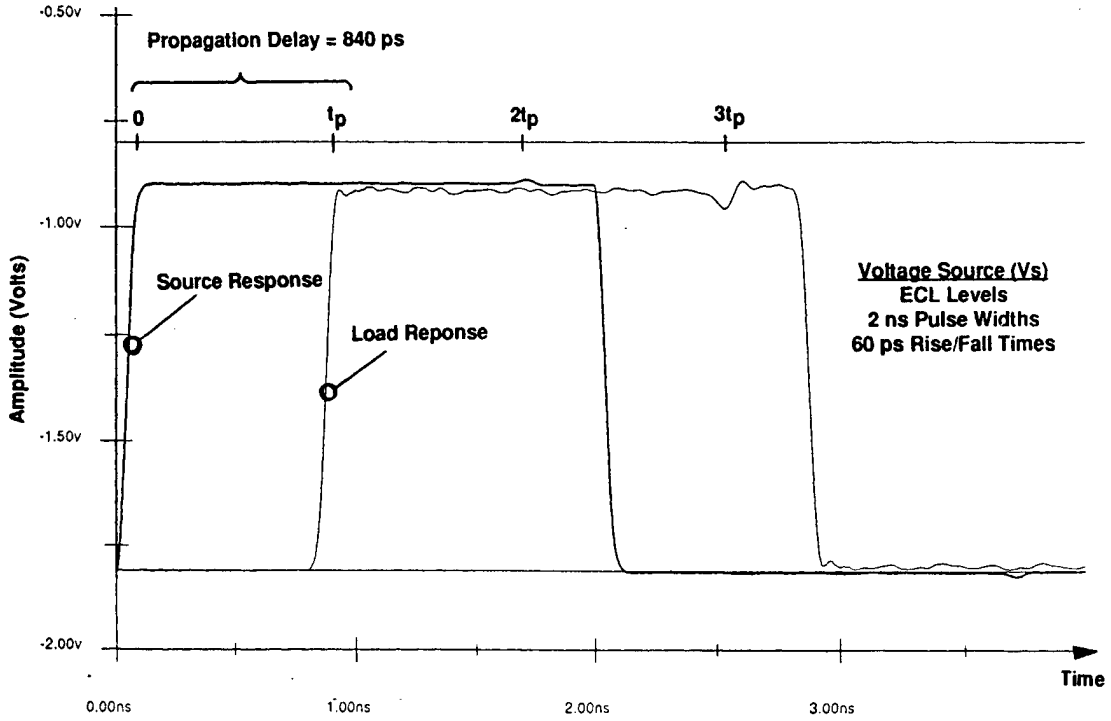

Figure 7. Time Domain Response for 2ns Pulse with 60ps Rise Time

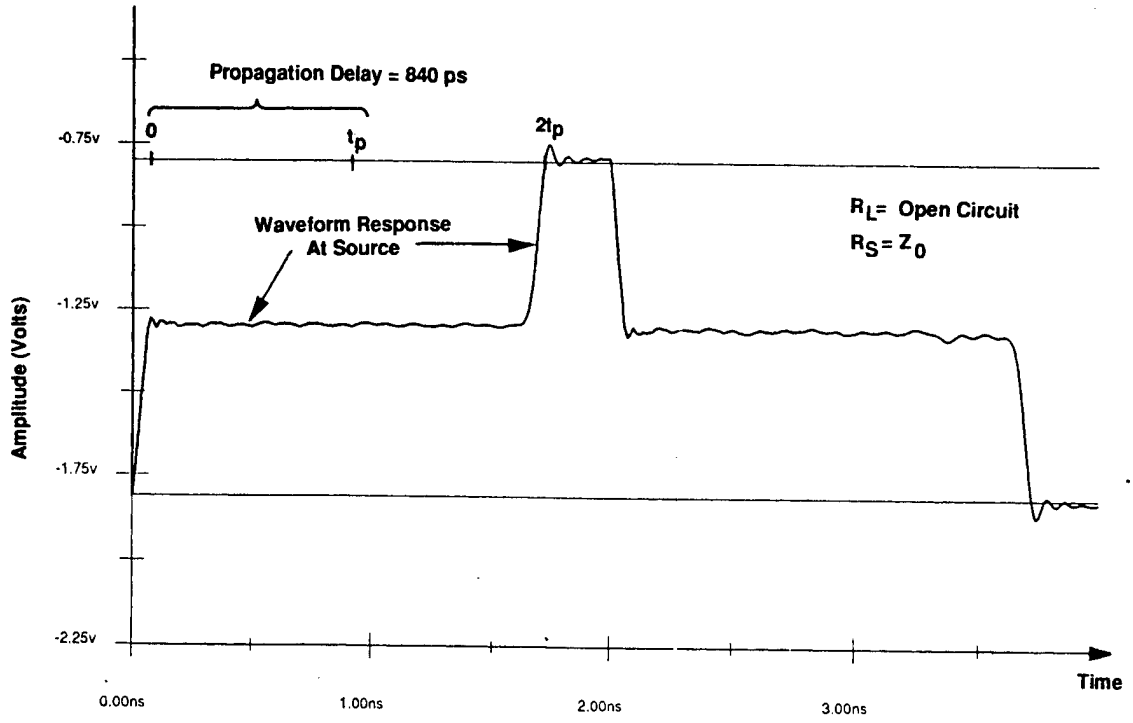

Figure 8. TDR Response for 40 Cell MCM Structure

References

1. R. C. Eden, "Application of Synthetic Diamond Substrates for Thermal Management of High PerformanceElectronic Multi-Chip Modules, "*Applications of Diamond Films and Related Materials*, Y. Tzeng, M. Yoshikawa, M. Murakawa, and A. Feldman, eds. (Elsevier Science Publishers B.V., Amsterdam, 1991), pp. 259-266.

2. G. Lu, K. J. Gray, E. F. Borchelt, L. K. Bigelow and J. E. Graebner, "White CVD Diamond for Thermal and Optical Applications." [to be Published in *Proceedings of Diamond 1992 Conference*, August 31 - September 2, 1992; Heidelberg, Germany]

3. The CTE of a large Norton CVD diamond slab sample was measured by G. Lu at Norton Diamond Film using a Theta dilatometer.

4. Quad XFX (transmission line parameter analysis) and XNS/TLC (transient analysis) software programs are copywrite CAD tools of Quad Design Technology, Inc.

5. Private communication between Don Marshall and Richard Eden with extensive improvements made by Eve Shen.

Acknowledgment

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APPENDIX B

Thermal Analysis of 3-D Diamond MCMs: Comparison with Experimental Measurements

This analysis was performed by Dr. Richard C. Eden

of Technology Applications

Raytheon Systems Company-Garland wish to thank Dr. Eden for his interest and continuing support to this program

Thermal Analysis of 3-D Diamond MCM: Comparison With Experimental Measurements

Richard C. Eden
Technology Applications

Summary of Results:

The goal of this portion of the effort was to carefully model the 3-D Diamond MCM structure and use that model to obtain the critical operating parameters obtained for the spray-cooled structure. The principal unknown parameters to be evaluated by this method include the heat transfer coefficient, H, obtained at the spray-cooled diamond cooling fins at the edge of the diamond substrate MCMs, the die attach thermal resistance, R_{th}(die) , and the lateral thermal conductivity, k, of the diamond substrate itself. A further derived quantity is the effective thermal resistance of the spray cooling fins, $R_{th}(L_c)$, as measured by the temperature difference, T_{ref}-T_{sat}, between the base of the cooling fins and the coolant saturation temperature, T_{sat}, divided by the power into the fins. As will be discussed subsequently, a satisfactory thermal model was developed and values for these operating parameters derived by careful comparison between measured operating junction temperatures under different operating conditions of the 3-D diamond MCM. The best performance was obtained with the 3-D MCM operated at a 45° angle so that gravity assistance was available to avoid flooding of the spray cooling chambers. This was because the spray manifold was designed for a stack of six diamond substrate MCMs, whereas the actual stack measured had only three diamond substrate MCMs. Further, only four die on each MCM was powered in the measurements (plus the center clock die which was operated at lower power). The effect of this is to force all of the power to pass through four (instead of eight) die-substrate thermal resistance in parallel, raising junction temperatures for any given power level. As a consequence, the maximum power level evaluated was 304 Watts per MCM, instead of the 400 Watts per MCM nominal design value, which meant that instead of 6x400=2400 Watts module dissipation, we had a maximum of 3x304=912 Watts, with many measurements carried out at lower power levels. Under conditions where the actual power is far below the nominal design power, the spray cooling chamber may become flooded, with a type of jet impingement cooling obtained instead of true spray cooling. This was observed in the horizontal orientation (MCM substrates and fins horizontal) of the module, in which the excess liquid had to flow "up hill" to escape into the suction line. By tilting the MCM at a 45° angle with the suction outlets at the bottom, excellent operation was obtained with good heat transfer coefficient values.

The best-fit heat transfer coefficient value obtained for this work was H=1.15 W/cm^2°K (or 2018 BTU/HrFt^2°F) with the FC87 (or FC5070) (T_{sat}=31°C nominal) Fluorinert fluid supplied by ISR with the cooling system. This value seems very good for a geometry in which the angle between the spray and most of the sprayed diamond tab surface is quite low. At this H, the effective thermal resistance of the 2.32 inch wide by 0.306 inch long spray-cooled fins (from fin base to T_{sat}) was 0.129°K/Watt for each tab (0.0645 °K/W for the two tabs on each diamond MCM). Hence, at P=304 Watts, the base of the spray cooled diamond tabs was only T_{ref}-T_{sat} =19.6 °K above the fluid saturation temperature. The best fit value for lateral thermal conductivity of the z=1.00mm thick diamond substrate material was found to be k=1200 W/m°K, in excellent agreement with the values claimed by Norton Diamond Film for this material. Note that this k value is that obtained after the 7200 via holes were led through and all metallization and MCM processing was completed, which eliminated concerns that drilling and processing might seriously degrade the thermal performance of the diamond substrate material. The final critical thermal parameter evaluated was the die to substrate thermal resistance, R_{th}(die). The best-fit value obtained for this parameter was R_{th}(die) =0.55 °K/Watt. This is a rather high value for a 1 cm x 1cm chip in a thermally sensitive application, as it leads, for example, at the maximum power level tested of P=304 Watts per MCM or P=71.44 Watts in each of the four side chips, to a junction-to-substrate temperature rise of 39.3°K. Considering that the total temperature rise due to lateral heat flow through the z=1.0mm thick diamond substrate over the 33mm path from the cooling fin base to the hottest point on the MCM is only 47 °K, wasting nearly 40 °K in die attach thermal resistance is unsatisfactory. There is every reason to believe, however, that this could be greatly improved by optimizing the die attach technology. Other than the higher than desired R_{th}(die) values, however, the thermal results measured for the 3-D diamond MCM built in this program were very gratifying, and a clear demonstration of the viability of this 3-D diamond MCM concept.

Thermal Model Calculation Approach:

While a full discussion of all of the technical details of the thermal model would be too lengthy to include here, it is appropriate to discuss the key aspects, and then provide additional backup material which can be examined for details of the calculated approaches and results. There are three steps to the thermal modeling: 1) calculating the temperature at the base of the spray cooled heat sink fins, 2) calculating (by 2-D Poisson's equation simulation) the substrate temperature rise (due to lateral thermal conduction in the diamond) between the base of the fins and the various points of interest under the IC die, and 3) calculating the junction to substrate temperature rise and adding it to the substrate temperature to get the junction temperatures at the points on the IC die corresponding to the experimentally-monitored temperature diode points for comparison to the experimental data.

Calculation of Temperature at Base of Spray-Cooled Diamond Fins:

Two heat flow processes are taking place simultaneously within the spray-cooled diamond fins; lateral thermal conduction within the diamond, which leads to a temperature gradient in the fins, and heat transfer from the top and bottom surfaces of the fin from the spray cooling itself. Because this heat transfer to ambient is sensitive to the temperature difference between the fin and the saturation temperature of the fluid, T_{sat}, it is necessary to solve a differential equation to obtain the T(x) temperature distribution in the fin. For a diamond fin of uniform width, W, thickness, z, and thermal conductivity, k, the temperature gradient along the x direction in the fin (x=0 is taken at the base of the fin, where it meets the MCM) will be given by

$$dT(x)/dx=-P(x)/(kzW) \qquad \text{Eq. 1}$$

where P(x) is the heat flow (in Watts) conducting along the diamond fin at point x (where P(x=0)=P, the total power into the fin). The heat flow out of the diamond fin leads to a gradient in the power remaining in the fin. We assume a constant heat transfer coefficient, H, from spray cooling from a surface at temperature, T_s, such that in an area, A, the heat loss is given by

$$P_s = HA(T_s - T_{sat},) = HAT(x) \quad [\text{where } T(x)=T_s- T_{sat}] \qquad \text{Eq. 2}$$

This heat loss at a point, x, leads to a gradient in P(x) as

$$dP(x)/dx = -P_s(x) = -HAT(x) = -2HWT(x) \quad [\text{for two surfaces sprayed}] \qquad \text{Eq. 3}$$

where the factor of 2 comes from the fact that both the top and bottom surfaces of the fins are being sprayed. Differentiating Eq. 1 and substituting Eq. 3 for dP(x)/dx gives the differential equation for temperature distribution within the spray-cooled fin as

$$d^2T(x)/dx^2 = (2H/kz)T(x) \qquad \text{Eq. 4}$$

This differential equation has solutions of the form of growing or decaying exponentials (or their sum). For example, if the length of the fin, L_c, is infinite, only the decaying exponential solution meets the boundary condition of T=0 at x=infinity, so we have as the solution

$$T(x) = T(0)\exp(-x/L_{eff}) \qquad (\text{for } L_c >> L_{eff}) \qquad \text{Eq. 5}$$

Where the characteristic temperature attenuation length in the fin, L_{eff}, is given by

$$L_{eff} = \text{Sqrt}(kz/2H) \qquad \text{Eq. 6}$$

Using Eq. 5 for T(x) in Eq. 1 and evaluating at x=0 gives for the effective thermal resistance of the fin, $R_{th}(L_c=inf)$

$$R_{th}(L_c=inf) = T(x=0)/P = (1/W)(1/\text{Sqrt}(2Hkz)) \qquad (\text{for } L_c >> L_{eff}) \qquad \text{Eq. 7}$$

In fact, for the H, k and z values appropriate for the diamond 3-D MCMs in this work, the value of the characteristic temperature attenuation length in the fin, L_{eff}, is found to be 0.7223 cm, so Eq. 7 will not be very accurate when the fin length is only $L_c = 0.777$ cm. The math is slightly messier for this case as the T(x) solution is the sum of $\exp(-x/L_{eff})$ and $\exp(+x/L_{eff})$ terms. The result of the calculation for this finite L_c case is

$$R_{th}(L_c) = (1/W)(1/\mathrm{Sqrt}(2Hkz))[(1+\exp(-2L_c/L_{eff}))/(1+\exp(-2L_c/L_{eff}))] \quad \text{Eq. 8}$$

Since the exponential portion of this is just the reciprocal of the hyperbolic tangent, $1/\mathrm{Tanh}(L_c/L_{eff})$, and the first part is the same as Eq. 7, this can also be written

$$R_{th}(L_c) = 1/(W\mathrm{Sqrt}(2Hkz)\mathrm{Tanh}(L_c/L_{eff}) = R_{th}(L_c=\mathrm{inf})/\mathrm{Tanh}(L_c/L_{eff}) \quad \text{Eq. 9}$$

[Note that I have not seen this analysis published anywhere; it is a pretty handy expression for this type of heat loss problem, and for the evaluation of the analogous problem of calculating ohmic contact resistances for short contacts.]

In the 3-D diamond MCM thermal model calculation, the absolute temperature at the base of the spray-cooled diamond fins is calculated from the total MCM power, P, and the $R_{th}(L_c)$ value from Eq. 9 as

$$T_{ref} = T_s(x=0) = T_{sat} + P\,R_{th}(L_c) \quad \text{Eq. 10}$$

Where T_{sat}=31.0°C was taken for the FC87 Fluorinert fluid, and for a total W=11.786 cm spray cooling fin width with kz=1.20 W/°K and H=1.15 W/cm^2°K, a value of $R_{th}(L_c)$ = 0.0645 °K/Watt was obtained. Note that it is assumed here that the power density into the fin is uniform (in the y direction), which would make the temperature along the fin base constant. In fact, this is not precisely true in this case of diamond MCMs in which the cooling tab is somewhat narrower than the body of the MCM substrate. However, as long as this assumption is consistently carried into the 2-D Poisson's Equation analysis, the resulting error will be small except for points very near the edge of the fin. At the highest power level measured, P=304 Watts per diamond MCM, the temperature rise above saturation was $P\,R_{th}(L_c)$ = 19.6°K, or T_{ref} = 50.6°C at the base of the spray cooling fin for T_{sat}=31.0°C. At P=229 Watts per MCM, these are $P\,R_{th}(L_c)$ = 14.77°K and T_{ref} = 45.77°C.

Calculation of Temperature Distribution in Diamond MCM Substrate:

The lateral thermal conduction in the diamond MCM substrate from the powered IC chips to the spray cooling fins leads to temperature gradients in the diamond substrate. Because of the complex geometry of the heated chip and cooling fin/MCM shape, solving for the $\Delta T(x,y)$ temperature distribution (where $\Delta T = T_s - T_{ref}$) analytically (as was done for the fin region above) would be impractical. What was done was to write a 2-D Poisson's Equation solver in HiQ script that does a finite difference simulation of the problem. Because of the horizontal and vertical symmetry of the MCM substrate and chip locations, only 1/4 of the substrate needs be simulated. A 1.0 mm simulation mesh size was taken, so the 1/4 substrate is simulated with a 33 x 38 mesh, or 35 x 40 including boundary points. All of the boundaries are taken as insulating except for the portion of the side that is the base of the spray cooled fin (which is taken at a fixed reference temperature of ΔT=0). It is assumed that the chip power is uniformly applied over the area of the chips, and the enhancement of the lateral thermal conductivity of the diamond substrate due to the addition of the silicon IC chip on it is considered (although the effect is not ver large with a z=1.0 mm thick diamond substrate. For details of just how the calculation is carried out, you can refer to the program listing for the computer simulation included here.

The numerical values of temperature rise from the cooling fin base, $\Delta T(x,y)$, are shown in the two tables for the P=304 Watt (four side chips powered with 71.439 W and the center clock chip at 18.07 W) case and for the P=229 Watt (four side chips powered with 52.72 W and the center clock chip still at 18.07 W) case. These tables are useful to obtain the exact substrate temperature value at any point under any powered or un-powered IC chip. This data is also shown in the form of a "3-D" surface graph in Figures 1 and 2 for these two cases. The location of the cooling fin base (at ΔT=0) is indicated by the heavy line. The graph for the P=229 Watt case also shows the outline of the powered and un-powered IC die locations. Note that the maximum temperature rise is ΔT_{max}=35.71°K for P=229W or ΔT_{max}=47.41°K for the P=304W case.

Calculation of IC Junction Temperatures and Using Thermal Model for Parameter Fitting:

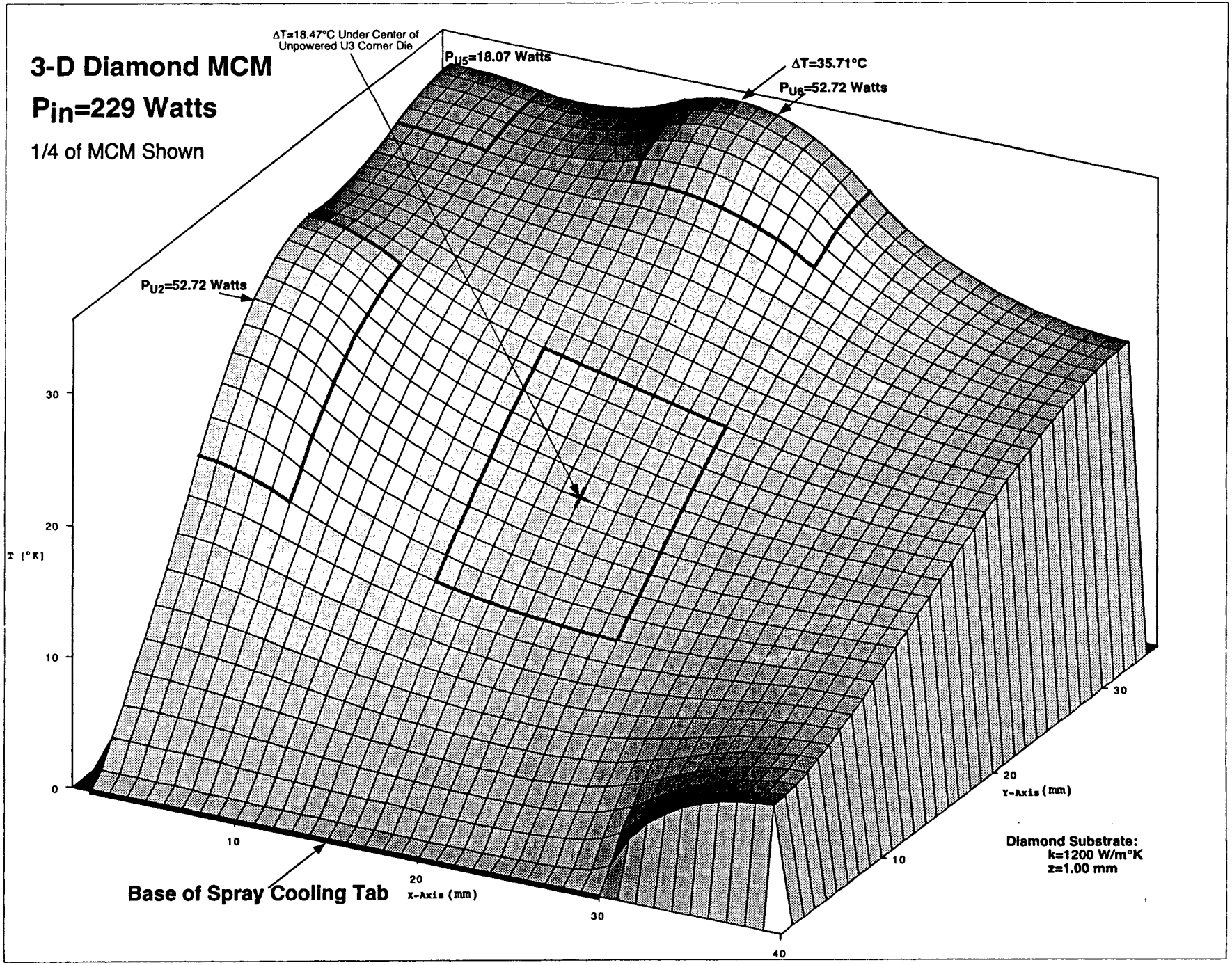
In both the 2-D Poisson's Equation simulation of $\Delta T(x,y)$ and in the calculation of the difference in temperature between the IC junctions (or thermal sensing diode) temperatures and the diamond substrate temperature underneath, it is assumed that the power dissipation is uniform over any given IC chip. It is also assumed that all IC chips have the same die attach thermal resistance, $R_{th}(die)$. Hence the absolute junction temperature at any point on an IC die will be given from

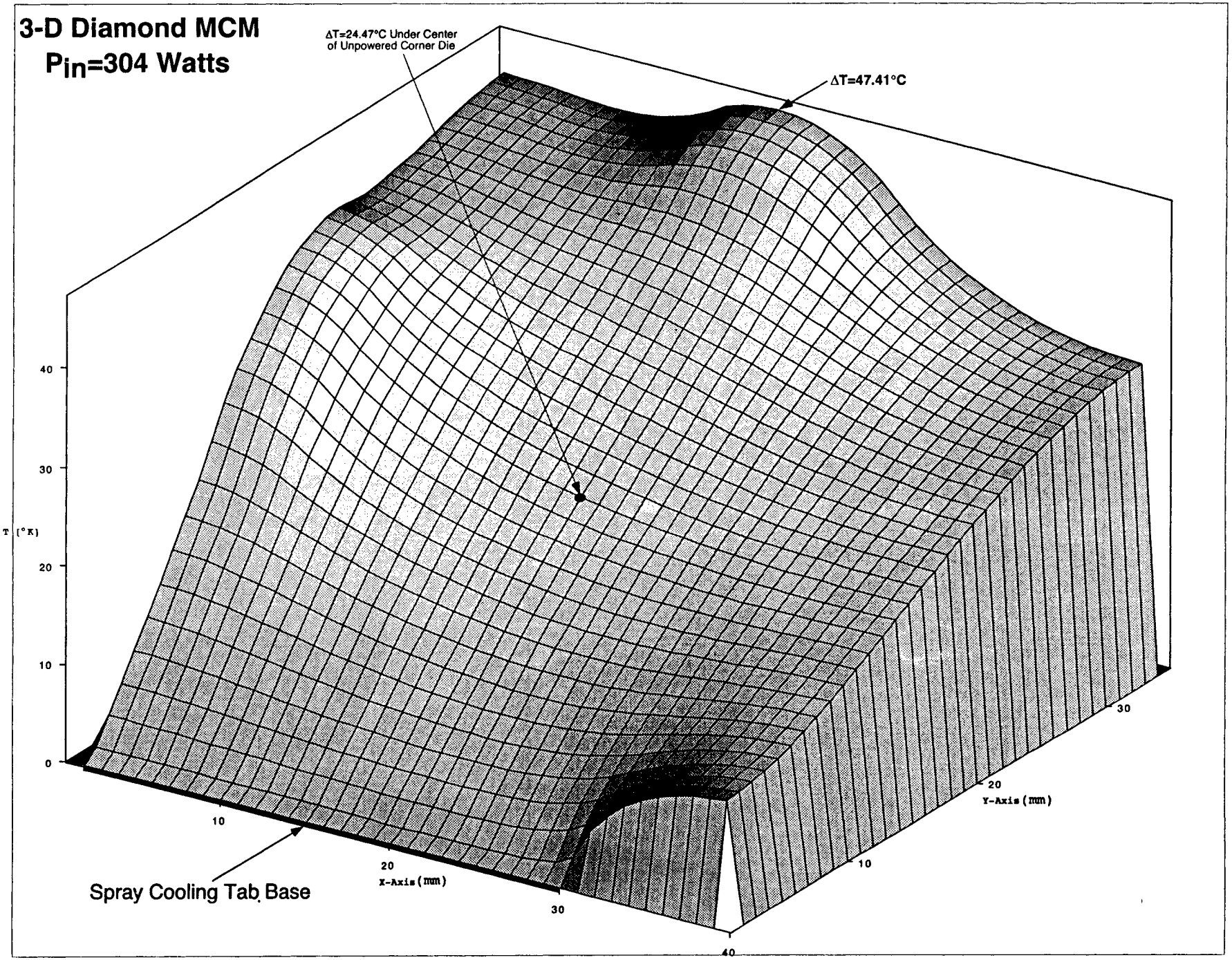
$$T_j(x,y) = T_{ref} + \Delta T(x,y) + P_{IC}\, R_{th}(die) \qquad \text{Eq. 11}$$

Where T_{ref} is obtained for the whole MCM from Eq. 10, $\Delta T(x,y)$ is from the 2-D thermal spreading calculation results as shown in the two figures or two tables, and the junction to substrate temperature rise is calculated for each chip based on its power dissipation, P_{IC}. For convenience, this entire calculation process has been put into an Excel 4.0 spreadsheet so that key parameters can be "twiddled to obtain best fit to the experimentally measured diode temperature data. The $\Delta T(x,y)$ data was put into the spreadsheet for the ten temperature sensing points used for this evaluation by looking up the diode location within the IC chip, and the location of the chip on the MCM, to obtain the x,y location of each diode. The $\Delta T(x,y)$ value for each location was either read from, or interpolated between data points in the $\Delta T(x,y)$ tables. The procedure was done separately for the two (P=229W and P=304W) cases.

Adjustment of the three critical parameters (H, $R_{th}(die)$ and k) to obtain the best overall fit of the experimental temperature data (also shown in the spreadsheet for comparison) for the two cases involves physical insight. The un-powered (U3) die data is independent of $R_{th}(die)$, and the U3 die is reasonably close to the spray-cooled fin, so this is a good place to focus for H adjustments. The clock die (U5) has only 25% of the power of the side chips in the 304 Watt case, so it is somewhat less sensitive to $R_{th}(die)$, and hence is a good place to look for k adjustments after a reasonably good $R_{th}(die)$ value has been obtained. (This particular diode gave somewhat erratic readings, however, so I wouldn't bet the farm trying to get precise agreement.) The $R_{th}(die)$ values are adjusted by looking at the heavily powered chips. The goal should be to get overall agreement. The Excel worksheet shown is my best effort in selecting these critical parameter values, and it shows the fitting accuracy obtained. For example, for P=229 W at the center of the un-powered (U3) die Tj=64.24°C was calculated, vs. 64.89°C measured, while for the 304 W case it was 70.24°C calculated vs. 73.54°C measured. In the 304 W case, the clock die was calculated at Tj=99.68°C but measured at 96.06°C and 100.75°C in two measurements only about a minute apart. Most of the measurements are within about ±4°C of the calculated values, although one particular diode consistently gave values around 10-12°C lower than expected (which might well be an experimental problem with this diode). In general, the quality of fit to the experimental temperature data is substantially better than expected when this work was undertaken.

As noted in the summary, the best-fit heat transfer coefficient value obtained for this work was H=1.15 $W/cm^2{}^\circ K$ (or 2018 $BTU/HrFt^2{}^\circ F$) with the FC87 (or FC5070) (T_{sat}=31°C nominal) Fluorinert fluid supplied by ISR with the cooling system. This value seems very good for a geometry in which the angle between the spray and most of the sprayed diamond tab surface is quite low. Hence, at P=304 Watts, the base of the spray cooled diamond tabs was only T_{ref}-T_{sat} =19.6 °K above the fluid saturation temperature. The best fit value for lateral thermal conductivity of the z=1.00mm thick diamond substrate material was found to be k=1200 W/m°K, in excellent agreement with the values claimed by Norton Diamond Film for this material. Note that this k value is that obtained after the 7200 via holes were led through and all metallization and MCM processing was completed, which eliminated concerns that drilling and processing might seriously degrade the thermal performance of the diamond substrate material. The final critical thermal parameter evaluated was the die to substrate thermal resistance, $R_{th}(die)$. The best-fit value obtained for this parameter was $R_{th}(die)$ =0.55 °K/Watt. This is a rather high value for a 1 cm x 1cm chip in a thermally sensitive application, as it leads, for example, at the maximum power level tested of P=304 Watts per MCM or P=71.44 Watts in each of the four side chips, to a junction-to-substrate temperature rise of 39.3°K. Considering that the total temperature rise due to lateral heat flow through the z=1.0mm thick diamond substrate over the 33mm path from the cooling fin base to the hottest point on the MCM is only 47 °K, wasting nearly 40 °K in die attach thermal resistance is unsatisfactory. There is every reason to believe, however, that this could be greatly improved by optimizing the die attach technology. Other than the higher than desired $R_{th}(die)$ values, however, the thermal results measured for the 3D diamond MCM built in this program were very gratifying, and a clear demonstration of the viability of this 3-D diamond MCM concept.


3-D Diamond MCM
Pin=229 Watts
1/4 of MCM Shown
ΔT=18.47°C Under Center of Unpowered U3 Corner Die
PU5=18.07 Watts
ΔT=35.71°C
PU6=52.72 Watts
PU2=52.72 Watts
T [°K]
0
10
20
30
10
20
30
40
X-Axis (mm)
Y-Axis (mm)
Base of Spray Cooling Tab
Diamond Substrate:
k=1200 W/m°K
z=1.00 mm


3-D Diamond MCM
Pin=304 Watts
ΔT=24.47°C Under Center of Unpowered Corner Die
ΔT=47.41°C
T (°K)
0
10
20
30
40
10
20
30
X-Axis (mm)
10
20
30
40
Y-Axis (mm)
Spray Cooling Tab Base

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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0	1.2252	3.6806	6.1518	8.6493	11.186	13.775	16.434	19.183	22.046	25.051	28.117	30.72	33.004	34.966	36.676	38.084	39.203	40.028	40.544	40.73	40.552	40.531	40.641	40.858	41.161	41.532	41.962	42.441	42.947	43.338	43.633	43.83	43.928	0
0	1.2148	3.6491	6.0974	8.5698	11.077	13.633	16.251	18.951	21.757	24.701	27.707	30.262	32.51	34.47	36.151	37.56	38.695	39.548	40.105	40.343	40.225	40.263	40.425	40.683	41.018	41.413	41.858	42.347	42.858	43.252	43.548	43.747	43.846	0
0	1.1998	3.6035	6.0191	8.4551	10.921	13.427	15.986	18.614	21.332	24.174	27.081	29.56	31.754	33.679	35.346	36.759	37.917	38.813	39.433	39.755	39.737	39.87	40.111	40.433	40.815	41.244	41.711	42.212	42.727	43.124	43.423	43.623	43.724	0
0	1.1809	3.5458	5.9202	8.3107	10.724	13.168	15.652	18.185	20.783	23.473	26.221	28.592	30.713	32.594	34.243	35.661	36.848	37.8	38.509	38.955	39.098	39.37	39.718	40.121	40.564	41.037	41.531	42.042	42.555	42.954	43.256	43.46	43.562	0
0	1.1588	3.4787	5.8053	8.1433	10.497	12.871	15.268	17.692	20.143	22.606	25.038	27.273	29.306	31.136	32.763	34.187	35.408	36.428	37.246	37.872	38.335	38.793	39.27	39.769	40.284	40.809	41.335	41.849	42.331	42.732	43.04	43.25	43.356	0
0	1.1345	3.4048	5.6792	7.9601	10.25	12.549	14.858	17.173	19.487	21.778	24.006	26.105	28.048	29.825	31.429	32.859	34.116	35.204	36.129	36.909	37.577	38.198	38.801	39.399	39.994	40.58	41.15	41.69	42.179	42.593	42.915	43.135	43.247	0
0	1.1087	3.3268	5.5464	7.7683	9.9925	12.218	14.441	16.657	18.853	21.011	23.103	25.093	26.958	28.686	30.269	31.704	32.994	34.142	35.158	36.058	36.867	37.619	38.337	39.033	39.711	40.368	40.995	41.58	42.104	42.547	42.893	43.13	43.25	0
0	1.0825	3.2472	5.4114	7.5743	9.7342	11.888	14.032	16.159	18.257	20.311	22.301	24.205	26.006	27.691	29.256	30.696	32.013	33.212	34.302	35.297	36.214	37.075	37.895	38.686	39.45	40.186	40.884	41.531	42.109	42.597	42.979	43.241	43.374	0
0	1.0563	3.1682	5.2779	7.3832	9.4815	11.569	13.641	15.69	17.705	19.676	21.586	23.421	25.168	26.819	28.367	29.81	31.15	32.392	33.543	34.613	35.618	36.57	37.483	38.365	39.218	40.04	40.823	41.551	42.203	42.755	43.185	43.48	43.63	0
0	1.0309	3.0916	5.1485	7.199	9.2396	11.266	13.273	15.253	17.199	19.1	20.946	22.725	24.428	26.048	27.582	29.028	30.386	31.662	32.863	33.996	35.073	36.106	37.103	38.072	39.016	39.934	40.817	41.647	42.398	43.033	43.528	43.865	44.036	0
0	1.0067	3.0186	5.0257	7.0247	9.0117	10.982	12.931	14.852	16.738	18.58	20.372	22.104	23.77	25.365	26.886	28.332	29.705	31.009	32.249	33.435	34.574	35.676	36.751	37.804	38.842	39.863	40.863	41.823	42.707	43.453	44.027	44.416	44.612	0
0	0.9841	2.9503	4.9111	6.8625	8.8004	10.72	12.617	14.485	16.319	18.112	19.857	21.549	23.183	24.755	26.264	27.709	29.093	30.418	31.692	32.92	34.111	35.275	36.419	37.553	38.683	39.814	40.948	42.076	43.156	44.042	44.713	45.161	45.385	0
0	0.9632	2.8876	4.8058	6.7138	8.6071	10.481	12.332	14.153	15.941	17.69	19.396	21.053	22.658	24.21	25.706	27.148	28.538	29.88	31.179	32.442	33.677	34.892	36.099	37.305	38.522	39.762	41.038	42.375	43.776	44.818	45.587	46.094	46.346	0
0	0.9444	2.831	4.7109	6.5796	8.4328	10.266	12.075	13.855	15.603	17.313	18.982	20.608	22.187	23.719	25.202	26.639	28.032	29.385	30.702	31.992	33.261	34.52	35.778	37.046	38.34	39.674	41.069	42.557	44.126	45.288	46.137	46.694	46.97	0
0	0.9278	2.7811	4.6271	6.4611	8.2786	10.075	11.847	13.59	15.301	16.976	18.613	20.209	21.764	23.276	24.745	26.175	27.566	28.924	30.254	31.562	32.857	34.148	35.446	36.763	38.117	39.523	41.007	42.599	44.272	45.517	46.427	47.024	47.319	0
0	0.9137	2.7385	4.5552	6.359	8.1451	9.9093	11.648	13.357	15.035	16.678	18.284	19.853	21.383	22.875	24.329	25.748	27.134	28.492	29.827	31.145	32.456	33.768	35.094	36.445	37.84	39.296	40.838	42.495	44.232	45.529	46.48	47.103	47.412	0
0	0.9023	2.7038	4.4964	6.2746	8.0336	9.7691	11.478	13.156	14.803	16.416	17.993	19.535	21.041	22.511	23.948	25.353	26.73	28.082	29.416	30.737	32.054	33.376	34.715	36.084	37.5	38.983	40.555	42.244	44.013	45.337	46.308	46.945	47.261	0
0	0.8938	2.678	4.4519	6.2095	7.9455	9.6558	11.337	12.988	14.605	16.189	17.738	19.253	20.734	22.182	23.599	24.987	26.35	27.691	29.017	30.333	31.647	32.967	34.306	35.677	37.095	38.58	40.155	41.848	43.619	44.946	45.919	46.557	46.873	0
0	0.8889	2.6626	4.4239	6.1659	7.8831	9.5714	11.228	12.852	14.441	15.996	17.517	19.005	20.459	21.883	23.278	24.646	25.991	27.317	28.628	29.931	31.232	32.54	33.866	35.221	36.622	38.087	39.638	41.304	43.051	44.356	45.313	45.94	46.25	0
0	0.8883	2.6594	4.4151	6.1471	7.8495	9.5186	11.152	12.75	14.312	15.838	17.33	18.789	20.216	21.614	22.984	24.329	25.652	26.957	28.248	29.53	30.81	32.096	33.396	34.721	36.086	37.507	39.007	40.615	42.305	43.563	44.484	45.087	45.386	0
0	0.893	2.6717	4.4299	6.1579	7.8492	9.501	11.112	12.684	14.217	15.714	17.176	18.605	20.003	21.372	22.715	24.033	25.331	26.61	27.876	29.132	30.384	31.637	32.9	34.182	35.492	36.848	38.267	39.781	41.375	42.557	43.421	43.987	44.268	0
0	0.905	2.7044	4.4752	6.2052	7.8886	9.5239	11.112	12.657	14.16	15.625	17.055	18.452	19.816	21.157	22.47	23.759	25.028	26.278	27.514	28.738	29.955	31.169	32.386	33.612	34.855	36.124	37.432	38.804	40.246	41.316	42.103	42.622	42.879	0
0	0.9276	2.7659	4.5611	6.2991	7.976	9.5935	11.157	12.67	14.14	15.571	16.966	18.329	19.662	20.967	22.248	23.506	24.743	25.961	27.163	28.351	29.529	30.698	31.863	33.027	34.192	35.361	36.534	37.703	38.83	39.747	40.438	40.9	41.13	0
0	0.9669	2.8705	4.7042	6.4543	8.1226	9.7177	11.25	12.728	14.16	15.553	16.91	18.235	19.532	20.803	22.049	23.273	24.476	25.66	26.826	27.975	29.11	30.232	31.341	32.439	33.525	34.595	35.641	36.645	37.568	38.344	38.94	39.343	39.546	0
0	1.0365	3.0449	4.9311	6.6912	8.3423	9.905	11.397	12.832	14.22	15.57	16.885	18.171	19.429	20.663	21.873	23.062	24.229	25.376	26.504	27.614	28.705	29.778	30.831	31.864	32.873	33.852	34.789	35.666	36.455	37.12	37.636	37.986	38.163	0
0	1.1706	3.3416	5.284	7.0371	8.6505	10.163	11.601	12.982	14.32	15.62	16.89	18.133	19.351	20.546	21.719	22.871	24.002	25.112	26.202	27.271	28.318	29.343	30.342	31.314	32.252	33.15	33.997	34.776	35.467	36.047	36.497	36.803	36.959	0
0	1.475	3.8668	5.8261	7.5227	9.0599	10.495	11.861	13.177	14.455	15.702	16.923	18.12	19.296	20.451	21.586	22.701	23.795	24.869	25.921	26.95	27.954	28.932	29.881	30.796	31.671	32.5	33.272	33.973	34.589	35.103	35.501	35.772	35.909	0
0	2.3375	4.8246	6.631	8.1677	9.5711	10.897	12.172	13.41	14.621	15.81	16.978	18.129	19.261	20.376	21.473	22.551	23.61	24.647	25.662	26.653	27.617	28.552	29.453	30.317	31.138	31.907	32.617	33.256	33.813	34.275	34.631	34.874	34.996	0
0	5.3879	6.463	7.7055	8.9461	10.16	11.349	12.518	13.671	14.811	15.938	17.053	18.155	19.244	20.32	21.379	22.421	23.445	24.448	25.428	26.383	27.309	28.204	29.063	29.882	30.655	31.375	32.033	32.622	33.132	33.552	33.876	34.095	34.206	0
0	7.3633	7.9339	8.782	9.7512	10.774	11.821	12.881	13.946	15.012	16.077	17.139	18.195	19.242	20.278	21.302	22.311	23.301	24.272	25.219	26.141	27.033	27.892	28.713	29.493	30.225	30.903	31.52	32.068	32.539	32.927	33.225	33.426	33.528	0
0	8.768	9.1274	9.7374	10.503	11.363	12.281	13.238	14.218	15.215	16.221	17.232	18.242	19.25	20.25	21.24	22.217	23.178	24.118	25.036	25.926	26.789	27.617	28.406	29.152	29.849	30.492	31.074	31.589	32.031	32.393	32.669	32.856	32.95	0
0	9.8133	10.07	10.537	11.16	11.893	12.704	13.57	14.475	15.408	16.36	17.324	18.294	19.265	20.232	21.192	22.14	23.074	23.988	24.88	25.745	26.58	27.38	28.142	28.859	29.528	30.142	30.696	31.185	31.602	31.943	32.203	32.379	32.467	0
0	10.602	10.803	11.182	11.707	12.346	13.071	13.863	14.704	15.583	16.487	17.41	18.344	19.283	20.222	21.155	22.079	22.989	23.88	24.75	25.593	26.405	27.183	27.921	28.615	29.26	29.852	30.384	30.851	31.25	31.575	31.822	31.989	32.073	0
0	11.189	11.357	11.681	12.14	12.711	13.373	14.107	14.897	15.73	16.596	17.485	18.389	19.302	20.216	21.128	22.031	22.922	23.795	24.648	25.471	26.265	27.025	27.745	28.421	29.047	29.621	30.135	30.587	30.971	31.284	31.521	31.681	31.762	0
0	11.607	11.756	12.045	12.461	12.986	13.602	14.294	15.046	15.846	16.682	17.545	18.426	19.318	20.214	21.109	21.997	22.872	23.731	24.568	25.38	26.16	26.906	27.612	28.275	28.888	29.448	29.95	30.39	30.764	31.068	31.298	31.454	31.532	0
0	11.877	12.015	12.283	12.673	13.169	13.756	14.421	15.148	15.925	16.741	17.586	18.452	19.33	20.214	21.097	21.974	22.84	23.689	24.517	25.319	26.09	26.827	27.524	28.177	28.782	29.333	29.827	30.26	30.627	30.925	31.151	31.303	31.38	0
0	12.009	12.142	12.401	12.778	13.26	13.834	14.484	15.199	15.965	16.771	17.608	18.465	19.336	20.214	21.091	21.963	22.823	23.668	24.491	25.288	26.055	26.788	27.48	28.129	28.729	29.276	29.766	30.195	30.558	30.853	31.078	31.228	31.304	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

304 Watts

2-D Finite Difference Simulation of Diamond 3-D MCM at 304Watts input per MCM Board
Calculation Grid is 1.00mm per Pixel
71.4384 Watts on each of the four Side chips
18.07 Watts on Center (Clock) Chip

Die Areas and Sprey Cooling Fin Edge Outlined
1/4 of MCM Shown (Calculation Symmetry)

Richard C. Eden 11/7/1998

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0.9253	2.7799	4.6465	6.5338	8.4513	10.41	12.423	14.505	16.675	18.952	21.271	23.246	24.982	26.491	27.782	28.86	29.723	30.365	30.777	30.945	30.846	30.867	30.993	31.204	31.488	31.832	32.231	32.678	33.155	33.522	33.796	33.979	34.07	0
0	0.9214	2.7678	4.6258	6.5035	8.4101	10.356	12.354	14.418	16.567	18.823	21.121	23.078	24.801	26.302	27.589	28.668	29.536	30.188	30.615	30.8	30.722	30.763	30.907	31.132	31.427	31.779	32.181	32.631	33.108	33.474	33.748	33.93	34.022	0
0	0.9136	2.7443	4.5854	6.4444	8.3294	10.25	12.218	14.246	16.353	18.562	20.817	22.739	24.434	25.918	27.196	28.278	29.158	29.831	30.287	30.51	30.474	30.558	30.738	30.992	31.308	31.674	32.085	32.538	33.015	33.379	33.652	33.834	33.925	0
0	0.9025	2.7103	4.5271	6.3591	8.2132	10.097	12.021	13.995	16.038	18.172	20.353	22.218	23.873	25.331	26.6	27.683	28.579	29.283	29.785	30.069	30.106	30.258	30.493	30.791	31.138	31.525	31.947	32.402	32.875	33.237	33.508	33.689	33.779	0
0	0.8884	2.6674	4.4536	6.2517	8.067	9.9052	11.773	13.677	15.63	17.651	19.715	21.5	23.101	24.527	25.782	26.868	27.784	28.529	29.095	29.469	29.623	29.875	30.186	30.54	30.928	31.342	31.776	32.229	32.691	33.046	33.314	33.494	33.584	0
0	0.8719	2.6175	4.3681	6.1271	7.896	9.6838	11.487	13.311	15.154	17.009	18.836	20.522	22.058	23.445	24.684	25.773	26.714	27.507	28.154	28.659	29.047	29.433	29.836	30.257	30.692	31.138	31.587	32.029	32.447	32.793	33.059	33.24	33.331	0
0	0.8538	2.5625	4.2742	5.9908	7.7139	9.4445	11.182	12.925	14.667	16.392	18.071	19.655	21.125	22.472	23.692	24.786	25.752	26.594	27.318	27.935	28.472	28.975	29.468	29.958	30.447	30.931	31.404	31.854	32.264	32.611	32.881	33.065	33.158	0
0	0.8347	2.5044	4.1753	5.848	7.5225	9.1979	10.872	12.541	14.195	15.822	17.4	18.903	20.314	21.624	22.829	23.925	24.914	25.799	26.588	27.292	27.931	28.526	29.102	29.66	30.206	30.736	31.244	31.718	32.145	32.506	32.788	32.981	33.079	0
0	0.8151	2.4451	4.0747	5.7034	7.33	8.9525	10.568	12.17	13.752	15.301	16.803	18.242	19.605	20.883	22.073	23.171	24.179	25.101	25.943	26.715	27.431	28.105	28.751	29.375	29.98	30.563	31.117	31.631	32.091	32.48	32.784	32.993	33.098	0
0	0.7956	2.3862	3.9751	5.5609	7.1417	8.7146	10.276	11.82	13.34	14.827	16.27	17.657	18.96	20.231	21.408	22.507	23.531	24.482	25.367	26.194	26.971	27.711	28.422	29.11	29.776	30.418	31.03	31.599	32.108	32.539	32.876	33.106	33.223	0
0	0.7766	2.329	3.8786	5.4235	6.9611	8.4883	10.001	11.495	12.962	14.397	15.791	17.137	18.426	19.655	20.819	21.919	22.955	23.931	24.85	25.721	26.55	27.347	28.117	28.865	29.595	30.304	30.985	31.626	32.204	32.693	33.074	33.334	33.465	0
0	0.7585	2.2745	3.7869	5.2934	6.7909	8.2764	9.7457	11.195	12.617	14.009	15.362	16.672	17.933	19.142	20.296	21.395	22.44	23.435	24.383	25.29	26.162	27.008	27.832	28.64	29.436	30.218	30.982	31.715	32.388	32.955	33.393	33.689	33.839	0
0	0.7418	2.2235	3.7012	5.1721	6.6329	8.0804	9.511	10.92	12.304	13.658	14.977	16.256	17.492	18.683	19.827	20.925	21.976	22.985	23.956	24.892	25.802	26.69	27.564	28.428	29.289	30.15	31.01	31.863	32.678	33.347	33.853	34.192	34.361	0
0	0.726	2.1765	3.6225	5.0606	6.4882	7.9016	9.2973	10.672	12.021	13.342	14.63	15.883	17.097	18.272	19.406	20.5	21.555	22.574	23.562	24.523	25.462	26.387	27.304	28.22	29.143	30.081	31.045	32.05	33.099	33.881	34.458	34.839	35.028	0
0	0.7119	2.1341	3.5514	4.9603	6.3577	7.7403	9.1048	10.448	11.767	13.058	14.319	15.548	16.742	17.901	19.025	20.113	21.169	22.195	23.195	24.174	25.137	26.092	27.045	28.006	28.983	29.988	31.037	32.152	33.324	34.193	34.829	35.246	35.453	0
0	0.6995	2.0967	3.4885	4.8714	6.242	7.5971	8.9336	10.249	11.54	12.805	14.041	15.247	16.423	17.566	18.678	19.76	20.814	21.842	22.85	23.841	24.821	25.798	26.779	27.774	28.794	29.851	30.964	32.154	33.402	34.331	35.01	35.456	35.677	0
0	0.6889	2.0647	3.4346	4.7948	6.1417	7.4724	8.7839	10.074	11.34	12.58	13.793	14.978	16.134	17.262	18.362	19.435	20.483	21.511	22.521	23.518	24.509	25.5	26.5	27.518	28.566	29.659	30.813	32.05	33.344	34.311	35.019	35.484	35.714	0
0	0.6803	2.0387	3.3904	4.7313	6.0579	7.3669	8.6557	9.9223	11.165	12.382	13.573	14.737	15.875	16.986	18.072	19.134	20.174	21.197	22.204	23.202	24.196	25.193	26.202	27.232	28.295	29.405	30.58	31.84	33.156	34.142	34.865	35.34	35.575	0
0	0.674	2.0193	3.3569	4.6823	5.9915	7.2815	8.5499	9.7949	11.015	12.211	13.38	14.524	15.642	16.735	17.806	18.854	19.884	20.897	21.897	22.89	23.881	24.875	25.883	26.912	27.975	29.087	30.263	31.524	32.841	33.828	34.553	35.028	35.263	0
0	0.6703	2.0076	3.3358	4.6494	5.9444	7.2177	8.4674	9.6921	10.891	12.065	13.212	14.335	15.433	16.508	17.561	18.594	19.609	20.609	21.598	22.58	23.561	24.545	25.541	26.559	27.608	28.703	29.861	31.102	32.4	33.371	34.082	34.549	34.78	0
0	0.6698	2.0052	3.3291	4.6351	5.9189	7.1776	8.4096	9.6149	10.793	11.944	13.07	14.171	15.248	16.303	17.337	18.351	19.349	20.333	21.306	22.273	23.236	24.203	25.179	26.173	27.195	28.257	29.376	30.574	31.83	32.765	33.45	33.898	34.12	0
0	0.6733	2.0144	3.3402	4.6431	5.9185	7.1641	8.3794	9.5647	10.721	11.85	12.953	14.031	15.085	16.118	17.131	18.126	19.104	20.068	21.022	21.967	22.909	23.851	24.799	25.76	26.741	27.754	28.813	29.94	31.125	32.003	32.646	33.067	33.276	0
0	0.6823	2.039	3.3741	4.6785	5.9478	7.1809	8.3788	9.5434	10.677	11.782	12.86	13.914	14.944	15.954	16.944	17.916	18.872	19.814	20.744	21.666	22.581	23.493	24.407	25.326	26.256	27.204	28.181	29.203	30.275	31.071	31.656	32.042	32.234	0
0	0.6993	2.0853	3.4387	4.7491	6.0134	7.233	8.4116	9.5531	10.662	11.74	12.792	13.82	14.825	15.809	16.774	17.722	18.654	19.572	20.476	21.37	22.256	23.134	24.006	24.88	25.753	26.627	27.503	28.374	29.213	29.896	30.411	30.755	30.926	0
0	0.7289	2.164	3.5464	4.8658	6.1235	7.3262	8.4813	9.5959	10.676	11.725	12.749	13.748	14.726	15.683	16.623	17.545	18.451	19.342	20.219	21.084	21.937	22.779	23.612	24.435	25.248	26.048	26.83	27.579	28.268	28.846	29.29	29.59	29.741	0
0	0.7813	2.2953	3.7172	5.044	6.2886	7.4668	8.5916	9.6735	10.72	11.737	12.729	13.696	14.646	15.576	16.488	17.383	18.262	19.126	19.975	20.809	21.629	22.435	23.225	24	24.756	25.488	26.188	26.844	27.433	27.929	28.314	28.575	28.707	0
0	0.8824	2.5188	3.9829	5.3045	6.5207	7.6607	8.7447	9.7862	10.794	11.775	12.732	13.668	14.586	15.486	16.37	17.238	18.089	18.925	19.745	20.548	21.336	22.105	22.855	23.584	24.287	24.959	25.593	26.175	26.691	27.124	27.46	27.689	27.805	0
0	1.1117	2.9145	4.3913	5.6702	6.8288	7.9107	8.9404	9.9324	10.896	11.835	12.755	13.657	14.543	15.414	16.268	17.108	17.932	18.74	19.531	20.305	21.06	21.794	22.506	23.193	23.849	24.47	25.047	25.572	26.033	26.417	26.714	26.916	27.019	0
0	1.7617	3.6362	4.9977	6.156	7.2138	8.2129	9.1736	10.107	11.02	11.916	12.796	13.663	14.516	15.356	16.182	16.994	17.791	18.571	19.335	20.079	20.804	21.506	22.183	22.831	23.447	24.024	24.555	25.034	25.45	25.796	26.062	26.243	26.335	0
0	4.0606	4.8708	5.8074	6.7424	7.6573	8.5534	9.4345	10.303	11.162	12.011	12.851	13.682	14.503	15.312	16.11	16.895	17.665	18.42	19.157	19.875	20.571	21.243	21.888	22.503	23.083	23.623	24.116	24.557	24.939	25.254	25.496	25.66	25.743	0
0	5.5492	5.9793	6.6185	7.3489	8.1196	8.9089	9.7073	10.51	11.313	12.116	12.916	13.711	14.5	15.28	16.051	16.81	17.556	18.286	18.999	19.691	20.362	21.007	21.625	22.21	22.759	23.267	23.73	24.141	24.494	24.785	25.007	25.158	25.234	0
0	6.6077	6.8786	7.3383	7.9152	8.5632	9.2554	9.976	10.715	11.466	12.224	12.985	13.746	14.505	15.258	16.004	16.739	17.462	18.17	18.86	19.53	20.178	20.8	21.392	21.953	22.476	22.958	23.395	23.781	24.112	24.383	24.591	24.731	24.801	0
0	7.3953	7.589	7.9411	8.4103	8.9627	9.5736	10.226	10.908	11.611	12.328	13.054	13.785	14.516	15.244	15.967	16.681	17.383	18.071	18.741	19.392	20.02	20.621	21.193	21.732	22.234	22.695	23.111	23.477	23.79	24.046	24.241	24.373	24.439	0
0	7.9893	8.1409	8.4268	8.8223	9.3035	9.8503	10.447	11.081	11.742	12.424	13.119	13.822	14.529	15.236	15.938	16.634	17.318	17.989	18.643	19.277	19.888	20.472	21.027	21.548	22.033	22.477	22.876	23.227	23.526	23.769	23.955	24.08	24.143	0
0	8.4317	8.5586	8.8026	9.1485	9.5787	10.077	10.63	11.225	11.853	12.505	13.175	13.856	14.543	15.231	15.917	16.597	17.267	17.924	18.564	19.185	19.782	20.353	20.894	21.402	21.872	22.303	22.689	23.028	23.316	23.551	23.729	23.849	23.91	0
0	8.7471	8.8592	9.0772	9.3903	9.7856	10.25	10.771	11.338	11.94	12.57	13.22	13.883	14.555	15.229	15.903	16.571	17.23	17.876	18.506	19.116	19.703	20.263	20.794	21.292	21.752	22.173	22.55	22.88	23.161	23.389	23.562	23.678	23.737	0
0	8.9503	9.0539	9.2565	9.5498	9.9234	10.366	10.866	11.414	12	12.614	13.251	13.902	14.564	15.229	15.894	16.554	17.205	17.844	18.467	19.07	19.65	20.204	20.728	21.218	21.673	22.087	22.458	22.782	23.058	23.281	23.451	23.565	23.623	0
0	9.05	9.1496	9.345	9.629	9.9922	10.424	10.914	11.453	12.03	12.637	13.267	13.913	14.568	15.229	15.889	16.545	17.193	17.828	18.447	19.047	19.624	20.174	20.694	21.182	21.633	22.044	22.412	22.733	23.006	23.228	23.396	23.509	23.566	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

229 Watts

2-D Finite Difference Simulation of Diamond 3-D MCM at 229Watts input per MCM Board
Calculation Grid is 1.00mm per Pixel
52.72 Watts on each of the four Side chips
18.07 Watts on Center (Clock) Chip

Die Areas and Sprey Cooling Fin Edge Outlined
1/4 of MCM Shown (Calculation Symmetry)

Richard C. Eden 11/7/1998